Photonics for Next Generation & Optical Computing

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Chapter 1 Introduction

1.1 Overview

This document expands on the state-of-the-art overview of photonics for next-generation computing, with a focus on optical computing and the full value chain—from technologies and platforms to design, packaging, test and characterization, and the most promising applications.

It covers Chapter 1's identification of the main drivers behind recent research developments; Chapter 2's review of the underlying Photonic Integrated Circuit platforms, the building blocks that can be developed on each platform, and a comparative view of performance and suitability, including packaging, testing, and reliability challenges. Chapter 3 analyzes the optical interconnects and light coupling mechanisms into and out of PICs, the introduction of Co-Packaged Optics with its significant use-cases in networks and HPC, its coexistence with traditional pluggables, and the requirements for next-generation data centers and HPC clusters. Chapter 4 provides a concise introduction to neuromorphic photonics, combining brain-inspired processing with ultrafast light and delay-based photonic reservoir computing on silicon and their applications. Chapter 5 gives an overview of quantum optical computing—from quantum computing fundamentals and photonic qubit encoding to linear-optical quantum computing (LOQC), integrated quantum photonics, quantum error correction, and the main quantum algorithms and applications. Chapter 6 reviews the most popular design and simulation tools used by the photonics community, categorized by solver approach and problem domain, plus the main metrics for quantifying PIC performance during test and characterization. Chapter 7 discusses three representative applications in terms of impact: HPC/AI acceleration in traditional workloads, photonics-enabled communications (including quantum key distribution) across data centers and beyond and sensing with a focus on LIDAR and the potential cost savings from photonic processing. Chapter 8 reviews the emergent materials and their role in heterogeneous integration of PICs, EICs, and other packaging components, the rise of software-defined and programmable photonics devices with key market players, standardization efforts, and Fraunhofer-related activities. Finally, Chapter 9 gives the conclusions and outlook, highlighting anticipated maturation and potential commercialization of photonic computing technologies in the coming years.

1.2 What Is Optical Computing?

Optical computing refers to performing useful computational tasks with light as the information carrier inside a system, not merely transporting bits between electronic processors. It encompasses photonic integrated circuits (PICs) and hybrid optoelectronic systems where some operations are executed in optical domain with the support of electronics components providing control mechanisms. Computation may be analog (continuous-valued) or digital (discrete), and it can be coherent, which includes the phase information, or incoherent, using only intensities.

Spatial, temporal, wavelength, and polarization degrees of freedom provide massive parallelism: matrices can be mapped to interferometer meshes or microring banks; convolutions arise from Fourier optics; correlations and transforms occur "at the speed of light." Because photons do not charge large capacitors, moving and mixing them can, in principle, be extremely energy efficient, with energy costs dominated by loss compensation, modulation, and detection rather than by wire charging.

The promise of optical computing is highest where linear operations dominate and where interconnect bandwidth is the bottleneck: machine-learning inference and training (matrix–vector and tensor contractions), signal processing (beamforming, filtering, correlation), scientific transforms (FFT), and certain optimization and sampling tasks. Its main challenges are precision (noise, drift, calibration), cascadability (loss and gain management), compact integration of sources and detectors, and co-design with memory and control.

Nonlinear behavior generated by gain saturation in optical amplifiers, the Kerr effect, or from optoelectronic conversion, can be used to implement activation functions for neural networks (NNs) in the optical domain.

Throughout this paper, we take a pragmatic view: “optical computing” includes any architecture in which light performs a nontrivial portion of the computation per unit energy, area, or time—whether the system is fully optical or tightly coupled to electronics.

1.3 Historical Milestones and Current Drivers

Optical computing has cycled through waves of innovation aligned with advances in light sources, modulators, and fabrication techniques. Early milestones in the 1960s–1980s established the foundations of analog optical processing: 4f correlators and matched filters executed image recognition and convolution at video rates; acousto-optic devices enabled beam steering and time–frequency manipulation; spatial light modulators brought programmability to holographic setups. These systems showcased breathtaking parallelism but were constrained by bulk optics, alignment sensitivity, and limited programmability and precision, and they receded as digital electronics improved [2] [3] [4] [5] [6].

The rise of fiber communications, matured lasers, detectors, and modulators, laying the groundwork for integrated photonics. Interferometer meshes for universal linear optics and compact resonator weight banks demonstrated how to map matrices to chips [7]. Heterogeneous integration of III-V gain on silicon and advances in thin-film lithium niobate and silicon nitride improved loss, bandwidth, and stability. In parallel, neuromorphic and nonlinear photonics explored lasers and resonators as dynamical elements for spiking, reservoir computing, and optimization.

The current momentum is fueled by three converging drivers. First, AI and data analytics demand orders of magnitude more linear algebra per joule and square millimeter. Transformers push memory bandwidth and interconnect energy costs to the forefront. Optical computing can potentially address this by executing large linear transforms in situ and by providing high-bandwidth, low-loss fan-out via wavelength and space. Second, packaging and systems trends like Co-packaged optics, chiplets, and advanced 3D integration make it practical to place photonics next to compute and memory, shortening links and amortizing overheads. Third, foundry ecosystems now offer repeatable photonic processes, device libraries, and design kits, enabling larger, more complex prototypes and making calibration and control part of the standard toolchain.

As the field moves from demonstrations to deployable accelerators, milestones will hinge on end-to-end performance in realistic workloads, robustness under drift and temperature, and manufacturable integration of sources, modulators, and detectors on economically viable platforms.

1.4 Scope, Terminology, and Notation

This paper takes a broad view of optical computing that includes any system that uses light to perform computation, including analog optical processors (Fourier optics, correlation, holography),

integrated photonic logic, photonic neuromorphic or AI accelerators implemented in free-space or on-chip, and photonic quantum computers. We also included information about optical interconnects as they play an important role in the development of next-generation optical computing.

Linear optics are usually used for implementing mixing and weighting while nonlinearities can supply thresholding, gain control, wavelength translation, or entangling operations. Coherent processors use phase and interference while incoherent processors use solely intensities. Information is usually encoded in amplitude, phase, wavelength, time, space, and polarization, with quantum encodings adding time-bin, path, polarization, frequency-bin qubits, and continuous-variable quadrature.

Our focus is on integrated platforms and system co-design: silicon, silicon nitride, and III–V compounds. We analyze optical interconnects from on-chip to chip-to-chip and larger fabrics, emphasizing when low-energy fan-out, routing, pooling, and reductions effectively move computation into the network.

Notation follows standard linear algebra: bold vectors and matrices (x, y, A), with layers $y = f(Ax + b)$, and f implemented optically or electronically. For classical computes we report throughput (MAC/s, TOPS/W) and energy per operation; for interconnects we use data rate and energy per bit. Precision is expressed as effective bits and RMS error; interconnect quality by BER and eye margins. Link budgets consider source power, loss, OSNR, crosstalk, fan-out, and latency. Comparisons emphasize end-to-end efficiency, latency, precision, and scalability under realistic packaging and control constraints.

Chapter 2 Optical Platforms & Integration Technologies

This chapter gives an overview of the different underlaying platforms for Photonic Integrated Circuits, which Building Blocks can be developed using different platforms and a brief comparison of the performances and suitability of use of one or another photonic platform. Moreover, the challenges with the packaging of PICs or crucial aspects such as testing and reliability are being discussed.

2.1 Scaling PIC processes

Scaling PIC processes to 300 mm is important for the future to go hand in hand with CMOS scaling in general. The main drivers are datacom applications, with increasing data transfer and energy efficiency in data centers and meeting the requirements for the exponential growth of data traffic in applications like AI and high-performance computing. In the next 10-15 years, it will be inevitable to meet the requirements for low-cost, high-volume production [8]. The scaling of PICs goes hand in hand with emerging quantum technologies like quantum communication, sensing, and computing. Consequently, scalability towards VLSI-class integration (>10k components per die) are currently primary objectives in silicon photonics and optical quantum computing. However, the densification is limited by crosstalk. A mitigation includes system-level simulation using Multiphysics modeling [9] to predict and suppress parasitic coupling. Because waveguides typically cannot be narrowed much below ~400-500 nm, the most effective approaches for area scaling are compact optical I/O couplers and high-speed modulators.

2.1.1 Silicon Photonics Platforms

Various material platforms are employed and investigated ranging from the well-established silicon on insulator platform to lesser-known ones like III-V material based like InGaP or AlGaAs. While some platforms like SOI and SiN already show excellent CMOS compatibility and hence are suitable for future scaling, other platforms like $LiNbO_3$ exhibit excellent optical properties but remain a challenge for its inclusion in an efficient PIC value chain. Each platform has its special features and properties [10] [11], the most important ones for future integrated quantum photonics are:

- CMOS foundry compatibility/scalability
- Low losses/high fidelity
- Optical nonlinearities (2nd and/or 3rd order)
- Low cost
- High bandwidth

The advantages and disadvantages of the most common platforms are listed in Table 1 with a focus on CMOS compatibility. In the end, it will be a combination of different approaches and the platform, including their perks and tradeoffs, will be chosen based on their application.

Platform	Advantages	Disadvantages	CMOS Compatibility

Silicon (Si)/SOI	▪ Mature fabrication ▪ High index contrast ▪ Scalable ▪ Low cost	▪ Indirect bandgap (no efficient light emission) ▪ Nonlinear losses	Excellent
Silicon Nitride (SiNx)	▪ Low propagation loss ▪ Broad transparency (VIS to IR) ▪ Readily available in CMOS foundries	▪ Lower index contrast (larger devices) ▪ No active functionality ▪ High mechanical stress	Very good
Lithium Niobate ($LiNbO_3$)	▪ Excellent electro-optic and nonlinear properties ▪ Low loss ▪ Wide transparency	▪ Expensive ▪ integration only as bonded layer ▪ Toxicity concerns	Moderate
Polymers	▪ Flexible ▪ Low cost ▪ Easy processing	▪ Lower stability ▪ Higher losses	Moderate
Silicon Carbide (SiC)	▪ Wide bandgap ▪ Nonlinear optics ▪ Robustness	▪ Immature fabrication ▪ Limited foundry support	Moderate
Aluminium Nitride (AlN)	▪ Wide bandgap ▪ High nonlinear coefficients ▪ CMOS compatible	▪ Immature/challenging fabrication ▪ expensive	Moderate
Barium Titanate (BTO)	▪ High electro-optic (Pockels) coefficient ▪ High refractive index – strong optical confinement ▪ Very high HF bandwidth	▪ High complexity epitaxial growth on Si ▪ Low TRL integration ▪ Defects leading to high optical losses	Good (integrated as thin film)
Indium Phosphide (InP)	▪ Direct bandgap (efficient light sources) ▪ Active and passive devices	▪ Higher cost ▪ Complex fabrication ▪ Limited wafer size	Poor
Gallium Arsenide (GaAs)	▪ Direct bandgap ▪ High-speed modulation ▪ Nonlinear optics	▪ Expensive ▪ Less mature integration ▪ Toxicity concerns	Poor

Table 1 Comparison of most common PIC platforms regarding their advantages and disadvantages as well as their CMOS compatibility.

2.1.2 Silicon Based Photonic Platforms (SiPh, SiNx)

Silicon is historically the first material for integrated photonics as it is low cost and has reliable manufacturing. However, due to its lack of opto-electronic properties like an indirect band gap and optical loss due to two-photon absorption, the trend moves to other materials. Another CMOS compatible material is silicon nitride. SiN waveguides exhibit low propagation loss, often below 0.1

dB per meter [12], making them highly suitable for applications requiring long-distance photon transmission and high-fidelity quantum operations on a chip. The broad transparency window, stretching from the visible to the mid-infrared range, enables a wide variety of applications in both classical and quantum photonics. Furthermore, it allows for scalable and cost-effective manufacturing that leverages the existing infrastructure of the semiconductor industry. In contrast to silicon, SiN does not suffer from two-photon absorption at telecommunication wavelengths, which supports the use of higher optical powers in integrated devices, and its refractive index and geometry can be precisely tailored. Its third order nonlinear properties facilitate on-chip frequency conversion, which is important for interfacing different quantum systems. The SiN platform also supports the integration of complex quantum circuits, including beam splitters, phase shifters, and interferometers, all with minimal optical loss. These features have enabled silicon nitride to play a pivotal role in the realization of on-chip photon sources, such as the efficient generation of entangled photon pairs and optical frequency combs, which are crucial building blocks for quantum communication and computing on up to 300 mm wafer scale. Despite these advantages, certain challenges remain. Among these are the integration of active components, such as lasers and detectors. Another problem is the Si-H and N-H bonds that absorb in the telecommunication C-band and the high mechanical stress, which scales with the wafer size. These hurdles are currently addressed to unlock the full potential of silicon nitride-based photonic and quantum chips.

2.1.3 III-V Materials

III-V compound semiconductors underpin many of the active functions required for scalable optical computing. Their direct bandgaps enable efficient light emission and gain. Their high refractive indices support tight optical confinement [13]. Their strong, engineerable nonlinearities can enable wavelength conversion and all-optical signal processing [14] [15]. Epitaxial control over quantum wells and dots, combined with mature growth techniques such as Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) and distributed Bragg reflector (DBR) stacks, has produced a rich device library including lasers, semiconductor optical amplifiers (SOAs), modulators, and photodetectors [16] [17] [18]. These devices can complement low-loss dielectrics such as silicon nitride and the passive routing advantages of silicon photonics [19].

For optical computation, the ability to link stages and save energy depends on signal regeneration, thresholding, and compact, fast conversion between electrical and optical signals [20] [21]. III-V lasers provide on-chip coherent sources and frequency-comb pumps while SOAs deliver gain for loss compensation and can implement nonlinear transfer functions via saturation. Electro-absorption modulators (EAMs) deliver small footprints, low drive voltages, and high bandwidths suited to dense arrays [22]. Phase modulation is possible via the Pockels effect in non-centrosymmetric III-Vs and via plasma dispersion from carrier injection/depletion [23]. High-speed p–i–n and avalanche photodiodes (APDs) based on III-Vs provide sensitive detection for interfacing with electronics.

Integration strategies critically shape system performance. Heterogeneous integration via wafer- or die-level bonding can bring III-V gains directly onto silicon or silicon nitride photonics, using evanescent or butt-coupled tapers to minimize loss [24]. Monolithic growth of III-Vs on silicon is advancing but remains challenging due to lattice and thermal mismatches. Thermal management is a key constraint: III-Vs typically have lower thermal conductivity than silicon, so heat spreading, contact engineering, and micro-packaging are central for dense compute arrays [25]. Foundry ecosystems for InP-based photonic integrated circuits and maturing Si/III-V processes now support multi-project wafers and standardized components, facilitating design reuse at scale.

Representative materials and their roles:

- GaAs/AlGaAs: Primary platform for 850 nm sources, DBR mirrors, and nonlinear waveguides. Enable quantum wells and dots for low-threshold lasers and fast saturable absorbers [26].
- InP/InGaAsP: Primary platform for 1.3–1.55 µm lasers, SOAs, EAMs, and integrated receivers. It has a strong presence in the telecom ecosystem and presents mature PIC processes and is widely used in heterogeneous Si/III-V lasers.
- InGaAs: High-responsivity photodetectors and APDs in the near-IR. They are used in high-speed transceivers and receivers [27].
- Other III-V materials: GaN/AlN, GaSb/InAs, and AlGaInP are generally less mature and less widely used than GaAs- and InP-based platforms, but they fill important niches. GaN/AlN extends operation into the visible and UV and offers robustness for high-power photonics [28]. GaSb/InAs covers the mid-infrared for sources and detectors beyond telecom bands [29]. AlGaInP provides efficient devices in the red–orange visible range [30]. Although foundry access and integration workflows are more limited today, these materials broaden the accessible wavelength space and enable specialized functions that complement mainstream optical-computing platforms.

In sum, III-V materials supply the active, nonlinear, and gain elements that make optical computing practical: compact sources, fast modulators, amplifiers for cascadability, and efficient detectors. The dominant architectural trend is co-integration—leveraging III-Vs for what they do best while using silicon or silicon nitride for low-loss routing and dense passive functions. Continued progress in heterogeneous integration, thermal engineering, and variability control will determine how far III-V-enabled photonic processors can scale in throughput and energy per operation.

2.1.4 Others (Glass, Polymer, SiC, etc)

SiC or SiC-on-insulator is a promising material platform for PICs. It is suitable for harsh environments due to its large thermal conductivity and robustness. has a large bandgap of 0.4–5 µm and exhibits both second- and third-order nonlinearities, enabling applications such as second-harmonic generation and Kerr frequency combs [31].

AlN also presents a promising CMOS compatible material that can act as a basic platform [32] [33]. Its wide bandgap of 6.2 eV allows applications from mid infrared down to UV wavelength. Moreover, it exhibits high second order nonlinearities in addition to third order nonlinearities, making it an ideal candidate for optical quantum computing. However, this counts mainly for the crystalline type grown on sapphire. The more CMOS compatible version, which is fabricated by DC sputtering, exhibits a polycrystalline structure, leading to some more needed evaluation of this material.

Lithium niobate [34] on insulator (LNOI) is compelling for quantum photonics due to its strong second order nonlinearity, ultra-low-loss waveguides/resonators, high-speed modulation, and low-noise. However, CMOS compatibility remains challenging because LN is non-native to Si fabs which required special packaging approaches like heterogeneous packaging and their fabrication challenges especially in etching, coupling, and wafer level bonding still remain [35]. Despite the current challenges, the LNOI platform is currently growing, implementing lithium niobate as a bonded layer.

Polymer photonic platforms offer low-temperature, wafer-scale fabrication of low-loss waveguides via spin-coating and imprinting, with broad transparency (VIS-NIR), high thermo-optic coefficients for efficient phase tuning. Their mechanical flexibility and refractive-index tailoring suit board-level interconnects and heterogeneous integration with Si/SiN [36]. However, they suffer from a lack of

long-term thermal and humidity stability and higher propagation loss from absorption and sidewall roughness.

2.5 Photonic Integrated Circuits (PICs)

2.5.1 Passive Components

Most optical computing use cases can be framed as matrix-vector (or, more generally tensor) operations. Optical and neuromorphic processors lean on passive photonic circuitry to realize linear algebra at low energy, which can be used to implement optical AI accelerators. These devices can manipulate the phase, path length, or wavelength of the optical signals, while introducing limited added noise. Below we outline the most common passive building blocks and highlight their applications for optical matrix–vector multiplication, convolution, or spike propagation in optical NNs.

• Multimode Interferometers (MMIs)

MMIs can provide 1 × N and N × N splitters/combiners with < 0.3 dB excess loss across > 30 nm bandwidth. In optical NNs they broadcast the optical amplitude of one neuron onto a N-number of outputs. Conversely, when used as low-crosstalk combiners, they collect partial optical sums in convolutional or pooling layers before a nonlinear activation is applied [37].

• Mach–Zehnder Interferometers (MZIs)

An MZI can provide a tunable element with two 50/50 couplers connected by differential phase shifters. By combining different MZIs into meshes, one can create L × L unitary processors able to execute arbitrary linear transforms at THz rates. Such meshes are the workhorse for analog optical matrix–vector multiplication, instantly mapping an input vector encoded on multiple wavelengths or time slots to an output vector in a single propagation step. In neuromorphic photonics, cascaded MZI grids supply trainable weights whose values can be updated in real time, supporting online learning [37].

• Optical Ring Resonators (ORRs)

Ring resonators supply wavelength-selective weights that can be re-tuned thermo-optically or electro-optically. A bank of rings acting on a frequency-division multiplexed (FDM) bus simultaneously multiplies K wavelengths by K independent coefficients, enabling massively parallel weight banks for neuromorphic photonics using wavelength-division multiplexing [38]. Because each ring can store its weight in a static thermal or carrier bias, the array acts as a dense, analog memory that consumes zero static power once programmed. Their high-Q filtering property also supports spiking-domain computing, where the rings delay or shape optical spikes to emulate synaptic time constants [39].

• Bragg Gratings

Bragg gratings implement narrowband reflectors or dispersion compensators that shape the impulse response of spiking neural substrates. In optical convolution engines they realize tap-delayed lines—effectively multiplying past inputs by fixed coefficients to perform finite-impulse-response filtering in a single waveguide. For neuromorphic photonics, chirped gratings can stretch or compress optical spikes, providing a controllable synaptic delay critical for temporal coding schemes [40].

• Phase Shifters

Phase shifters can be used to calibrate MZI meshes, shift ORR resonances, and realize optical weights. Thermo-optic shifters offer large tuning ranges for coarse calibration, while carrier-induced or Pockels-effect shifters can provide sub-nanosecond updates, allowing rapid weight modulation during inference or learning [41]. Through careful co-integration of these passive blocks, a PIC can execute parallel, low-energy, and ultrafast linear operations.

2.5.2 Active Components

Purely passive photonic meshes are linear. In order to build a complete optical or neuromorphic computer one needs gain, modulation, and non-linear detection on the same chip. The following active devices deliver those capabilities while remaining compatible with commercial CMOS or heterogeneous III–V foundry flows.

• Semiconductor Optical Amplifiers (SOAs)

Heterogeneous InP-on-Si SOAs can provide 10–20 dB small-signal gain, 100 ps carrier lifetimes, and saturation powers >10 dBm. Placed after lossy interferometer meshes they can restore signal levels and, when biased near transparency, exhibit sigmoid-like gain compression that serves as an optical ReLU or spiking threshold, which is critical for implementing multi-layer photonic neural networks without optical-electrical-optical conversions [37].

• Electro-Optic Modulators

Carrier-depletion Si or GeSi modulators can reach 50–70 GHz bandwidth and can be used to input vectors from CMOS DACs into optical amplitudes or phases, while thin-film $LiNbO_3$ or $BaTiO_3$ Pockels modulators can enable ultrafast in-situ weight updates in analog training architectures [42]. Phase-Change Material (PCM) cells (e.g., GST on Si waveguides) offer non-volatile multi-level weights programmable with nJ pulses, mimicking synaptic plasticity in photonic memristor networks [43].

• Optical Switches

Optical switches can control the path and state of light in photonic circuits and act as core elements for routing, multiplexing, and implementing logic operations in optical computing. By switching purely in the optical domain, they enable ultrafast, low-latency processing and interconnects while reducing energy and avoiding costly electro-optic conversions.

• High-Speed Photodiodes

Ge-on-Si or UTC photodiodes integrated next to waveguides deliver >70 GHz 3 dB bandwidth, shot-noise-limited responsivity of 0.8 A W^{-1}, and dark currents <1 nA. In neuromorphic settings they convert summed optical currents into electrical currents for mixed-signal learning loops or external monitoring.

• Integrated Lasers

Distributed-feedback (DFB) or distributed Bragg reflector (DBR) lasers, heterogeneously bonded to Si, supply on-chip coherence with linewidths above 100 kHz. Local, low-noise sources minimize coupling loss and phase drift, allowing each weight bank or MZI mesh to operate autonomously inside a large-scale optical computer.

By tightly integrating these active elements alongside passive interferometric meshes, a photonic processor can perform different types of operations. The most important use of these components is

related to the introduction of nonlinear activation into the optical neural networks, as well the as the conversion and interaction between optical and electrical signals.

2.5.3 Testing, Packaging, and Reliability

Compared to electronic integrated circuits (ICs), PICs usually demand specialized packaging and testing due to their optical interfaces and their thermal sensitivity. These factors can make packaging and testing the dominant cost drivers of photonic modules, unlike in electronics where the chips themselves account for most of the cost [44].

PIC fabrication spans multiple technologies and materials but lacks standardized approaches for packaging, testing and reliability. Integration into a module typically involves wafer-level testing, chip dicing, optical coupling (to fibers or lasers), electrical interconnection with electronic ICs, and final packaging. This section explores these steps, highlighting the unique challenges, guidelines, and emerging technologies for next-generation modules such as photonic chiplets and photonic interposers. PICs require both optical and electrical interconnects to be tackled separately.

- Optical interconnects link on-chip waveguides to external ones, like for example optical fibers, while aiming to maximize coupling efficiency. Aligning multiple coupling points can be a very complex and costly process.
- Electrical interconnects provide signal connections, often at high data rates, between the PIC and external electronics. These can include RF lines that connect active devices such as modulators or photodiodes [45].

The integration of PICs into functional modules typically follows a sequence of critical steps: wafer-level test, chip dicing, optical and electrical interconnection, assembly with electronic ICs, and final module packaging. At each stage, the requirements for high-precision alignment, mode matching, and thermal stability significantly exceed those of conventional electronic packaging [46].

Wafer-Level test of PICs

Wafer-level testing is critical for identifying Known Good Dies (KGDs) prior to packaging, yet it presents challenges distinct from microelectronics due to the need for optical I/O access. Test strategies must therefore be adapted to the coupling structure of the PIC.

For silicon photonics, vertical grating couplers are most widely used, as they allow wafer-level probing by combining standard electrical probe stations with optical probes such as bare fibers or fiber arrays. High precision alignment (<1 µm) is required, typically achieved using multi-axis piezoelectric micro-positioners capable of real-time feedback control [47] [48]. Fiber arrays provide scalability and robustness but require additional rotational degrees of freedom for parallelism and polarization management.

Historically, edge couplers posed a challenge since they required diced chips for optical access. Recent advances, such as reflective glass probes (e.g., WAFT interfaces), enable wafer-level testing by integrating front-side cavities and angled reflectors to redirect light vertically, allowing measurement of dense waveguide arrays with >60 dB dynamic range [49] [50].

Electro-optic (E/O) characterization further extends test complexity. In addition to conventional electrical instruments, optical measurements involve tunable laser sources, wavelength meters, and broadband photodetectors. Advanced swept-laser techniques now enable rapid spectral acquisition (1 pm resolution over 100 nm in ~10 s), supporting comprehensive testing of passive and active

functions, including photodiodes, phase shifters, and RF modulators via Vector Network Analysis [51].

Packaging of PICs

Following wafer-level testing and KGD selection, PICs proceed to dicing, die attach, and electrical interconnection, where packaging becomes a critical step. The design of PIC packages requires a holistic approach addressing electrical-optical integration, thermal management, and mechanical stability across diverse materials [52] [53].

Key design steps include material selection, thermo-mechanical optimization, and RF performance tuning, all highly application dependent. For example, high-power modules demand efficient heat dissipation, while telecom or datacom systems may require hermetic sealing or adherence to standardized form factors. Thermo-mechanical stability is particularly critical, as thermal crosstalk and coefficient of thermal expansion (CTE) mismatches can degrade device performance. Typical solutions to these issues usually involve thermo-electric coolers (TECs) and thermistors.

In parallel, RF design ensures high-frequency signal integrity. This involves co-optimizing PCBs, interposers, and interconnects (wire bonds, bumps) using impedance-matched transmission lines to minimize losses, reflections, and crosstalk. Packaging design rules constrain channel density, line pitch, and connector impedance, balancing electrical and optical I/O requirements.

Ultimately, reliable PIC packaging requires iterative simulation (thermal, mechanical, RF) and validation through multi-stage testing, first at the module level, then on the fully integrated package.

Design rules for packaging and testing

Efficient automation of PIC wafer-level testing requires adherence to specific design rules for PIC testing early in the design process [54] [55] [56] [57]. These rules align with broader packaging design guidelines and are typically implemented using dedicated EDA layers, templates, and test scripts. Key considerations include:

- Die orientation and port placement: Ensures consistent alignment of optical and electrical interfaces. Templates in design software facilitate uniform die layouts.
- Keep-out zones: Required around optical probe areas (bare fiber or fiber arrays) to prevent mechanical interference with electrical pads. Similar zones are needed for RF probe access to enable simultaneous optical–electrical testing.
- Alignment and pitch: Standardizing pad orientation, optical port alignment, and inter-pad spacing simplifies automated handling and reduces wafer rotation during testing.

By integrating these rules during the early design phase, wafer-level testing becomes faster, more reliable, and compatible with automated testing systems.

Reliability of PICs

Optical interconnects require micron-scale alignment between on-chip waveguides and external fibers, and any misalignment or mechanical stress can lead to significant signal degradation and early-life failures [58] [59]. Electrical interconnects, particularly high-speed RF connections, are similarly susceptible to degradation from thermal cycling, mechanical stress, and impedance mismatches, which can compromise signal integrity and module longevity [60].

Advanced probing techniques, including vertical grating couplers and reflective glass probes, allow comprehensive electro-optic characterization before packaging, reducing the risk of embedding

defective dies into final modules [61]. The iterative combination of thermal, mechanical, and RF simulations during package design, coupled with multi-stage validation at both die and module levels, is essential for ensuring long-term operational reliability [62]. Furthermore, adherence to early design rules, such as standardized die orientation, port placement, and alignment tolerances, improves testing reproducibility and reduces assembly-induced stress, directly enhancing PIC lifetime [63] [64].

Emerging solutions, including thermoelectric stabilization, robust fiber arrays, and optimized packaging materials, are central to improving reliability and addressing the historically limited serviceability and testability of PIC modules [59]. As PIC deployment scales, particularly in data center and high-performance computing networks, the reliability of optical and electrical interconnects will remain a key determinant of overall system performance and cost-effectiveness.

Chapter 3 Optical Interconnects & Co-Packaged Optics

This chapter deals with the optical interconnects in photonics, where different light coupling mechanisms in-and-out of PICs are being described and analyzed with their advantages and disadvantages. The second part of the chapter introduces the co-packaged optics (CPO) topic which has received much attention from the photonics community lately. The most significant use-cases of CPO in the network, its advantages and its co-existence with the classic pluggables are being discussed here. The requirements and wish list for next generation datacenters and high-performance computing (HPC) clusters are also mentioned in this chapter.

3.1 On-Chip Optical Interconnects

Efficient light injection and extraction are fundamental to the performance and scalability of PICs, the main component of on-chip optical interconnects. A critical challenge is the mode size mismatch between high-index PIC waveguides, which is often sub-micrometer in silicon photonics, and standard single-mode optical fibers, which exhibit a mode field radius of approximately 5 µm. Without effective mode-matching strategies, this difference can result in high insertion loss, limiting the achievable bandwidth, power efficiency, and overall system performance [52] [46] [45].

To mitigate this mismatch, Spot Size Converters (SSCs) or equivalent mode-expanding structures are employed. SSCs facilitate adiabatic transformation of the optical mode from the submicrometric PIC waveguide to the larger fiber mode, therefore enhancing coupling efficiency. The following coupling architectures are widely adopted in on-chip optical interconnect systems, each offering distinct trade-offs in terms of bandwidth, loss, polarization sensitivity, and manufacturability:

Edge Couplers [65]

- Provide in-plane coupling at the chip facet.
- Incorporate SSCs such as 3D adiabatic tapers, inverted tapers, metamaterial-assisted tapers, or hybrid waveguides (e.g., SiN over tapered Si) to expand the guided mode for fiber compatibility.
- Strengths: Broad spectral bandwidth, low polarization-dependent loss (PDL < 1 dB).
- Limitations: Require high-quality facet preparation (cleaving, polishing or etching) and complicated wafer-level testing.

Vertical Grating Couplers (VGCs) [66]

- Employ diffractive gratings to couple light out-of-plane (≈82–90°).
- Strengths: Facilitate wafer-level testing, enable coupling to fiber arrays, and allow placement flexibility across the chip surface without facet processing.
- Limitations: Narrow bandwidth (<30 nm), sensitivity to polarization (partially mitigated by two-dimensional gratings), and insertion losses typically on the order of 3–4 dB.

Evanescent Couplers [65]

- Achieve coupling via mode overlap between a tapered PIC waveguide and an external waveguide placed in close proximity.
- Strengths: Broadband, with large alignment tolerance (>50 nm along the propagation axis).
- Limitations: Require precise taper optimization and accurate positioning, making manufacturability more complex.

Photonic Wire Bonds (PWB) [67]

- Utilize transparent polymer waveguide wire bonds to bridge the gap between nanophotonic circuits located on different chips.
- Its main advantage is the enabling of flexible optical multi-chip assemblies, challenging the current paradigm of highly-complex monolithic integration.
- Demonstrated overall losses of only 1.6 dB in multi-Terabit/s data transmission experiments.

Reconfigurable Spot Size Converters [68]

- Employ adjustable structures to dynamically match the mode sizes between the PIC and external fibers.
- Offer adaptability in coupling efficiency, accommodating variations in fiber dimensions or alignment tolerances.

Buried 3D Spot-Size Converters [69]

- Integrate multi-stage tapers within a buried waveguide structure to facilitate mode expansion.
- Provide low-loss coupling with reduced sensitivity to alignment errors.

Polymer-Based Spot Size Expanders [70]

- Utilize polymer materials to create SSCs that can be integrated onto the end face of a silicon chip.
- Demonstrated low coupling efficiencies, addressing the mode size mismatch between silicon photonic chips and single-mode fibers.

The continued advancement of PIC technology will depend on the development of scalable, high-yield packaging and test processes. Approaches such as photonic chiplets and photonic interposers hold promise for modularizing integration and reducing assembly costs, but their success will rely on robust optical coupling strategies and standardized interconnect platforms. Achieving same maturity level as the electronic integration in terms of cost efficiency and scalability remains a central challenge for the industrial adoption of photonic systems [52] [46] [45].

3.2 Co-Packaged Optics (CPO)

CPO represents a paradigm shift in data center and HPC infrastructures, integrating optical transceivers directly with switch ASICs or compute processors. By minimizing electrical trace lengths and relying on silicon photonics, CPO achieves higher bandwidth density, lower power consumption, and improved scalability, positioning it as a main component of next-generation cloud and AI architectures [71] [72] [73]. Unlike pluggable optics, which are constrained by power, density, and thermal limitations, CPO provides a scalable solution for both scale-out and scale-up network topologies.

The primary reason for CPO adoption is the explosive growth of AI workloads, particularly large language models (LLMs) and generative AI, which demand unprecedented bandwidth, energy efficiency, and low-latency interconnects [74]. Scale-out architectures benefit from CPO in the form of long-reach, high-bandwidth optical connections between racks, supporting Ethernet and InfiniBand fabrics in hyperscale data centers. Scale-up architectures, by contrast, exploit CPO to replace copper interconnects within GPU-to-GPU and node-to-switch fabrics, providing longer reach, higher connectivity, and superior energy efficiency for AI training and HPC clusters [75]. Early CPO deployments are expected to focus on these scale-up environments before expanding into scale-out fabrics as the technology matures.

Recent industry developments highlight the accelerating momentum of CPO. At GTC 2025, Nvidia introduced its Spectrum-X and Quantum-X silicon photonic switches, equipped with 1.6 Tbps ports and designed to connect millions of GPUs in large-scale “AI factories” [76]. By integrating CPO into its architecture, Nvidia overcomes the bandwidth and power limitations of traditional network switches, demonstrating the role of CPO as a key enabler of exascale AI infrastructures [77].

The key components of CPO are PICs, which combine lasers, modulators, photodetectors, and waveguides into compact platforms for electrical-to-optical conversion [78]. For scale-out networks, standardized PICs enable cost-effective interoperability for Ethernet switches, while customized PICs support proprietary interconnects such as Nvidia’s switch replacements, offering multi-terabit capacities through advanced modulation formats (PAM-4, NRZ) and dense wavelength-division multiplexing (WDM) [79].

The realization of CPO consists of multiple integration approaches, with trade-offs between scalability, thermal management, and optical performance. Edge-coupled designs are the preferred coupling scheme since they provide direct in-plane connections between the optical engine and the ASIC edge, often incorporating SSCs to match the high-index waveguides with optical fibers.

Bandwidth scaling in CPO is pursued through two complementary strategies. Scale-out emphasizes an increase in the number of optical engines per ASIC and higher per-lane speeds to maximize distributed throughput. Scale-up, on the other hand, focuses on increasing lane data rates and leveraging WDM to expand the capacity of individual channels, which is critical for dense, high-performance fabrics [80]. Both strategies are essential to meeting the escalating requirements of AI and HPC clusters.

A crucial aspect of these CPO architectures is photonic packaging, realized through either 2.5D or 3D integration. In 2.5D packaging, optical engines and ASICs are co-assembled on a silicon interposer or organic substrate, offering manufacturing maturity, improved signal integrity, and reduced parasitic effects [81]. However, scalability and thermal challenges limit its applicability in very high-density systems. By contrast, 3D integration vertically stacks optical and electronic components using through-silicon vias (TSVs) or silicon bridges (e.g., Intel’s EMIB), thereby reducing interconnect lengths, enhancing bandwidth density, and improving power efficiency [82]. Nevertheless, 3D packaging introduces fabrication complexity, higher costs, and stringent thermal management requirements.

The main performance metric in CPO is bandwidth density (Tbps/mm), also referred to as beachfront density, which quantifies the optical throughput per unit edge length of the ASIC die, photonic chiplet, or optical engine [83]. Maximizing this metric allows more optical bandwidth to escape from the chip without increasing footprint or power consumption, directly addressing the space and energy constraints of hyperscale data centers.

More advanced and complex solutions push beyond edge-coupled designs by employing photonic interposers as optical “motherboards.” These large-scale substrates, often several times reticle size, integrate lasers, waveguides, and optical switching/routing elements while hosting compute and memory chiplets in stacked 3D configurations [84]. By providing extended optical I/O surfaces, photonic interposers dramatically enhance effective bandwidth density, reduce latency, and simplify system integration, making them a promising candidate for next-generation HPC and AI data center architectures, the drawback is the complexity on the packaging side and thermal management.

3.3 Datacenter and HPC Optical Networking

Optical interconnects are the central component to both modern data center and high-performance computing (HPC) architectures, driven by the rapid expansion of cloud services, artificial intelligence (AI) workloads, and large-scale scientific simulations [85] [86] [87]. Traditional copper interconnects are constrained by limited bandwidth, high power consumption, and thermal challenges, motivating the adoption of optical technologies for both intra-rack and inter-rack communication.

In hyperscale data centers, optical networking supports high-bandwidth, low-latency connectivity between racks, pods, and clusters. Common implementations include Ethernet and InfiniBand fabrics, enhanced with dense wavelength-division multiplexing (DWDM) and advanced modulation schemes such as PAM-4 to maximize spectral efficiency and link throughput while reducing energy per bit [88]. Scale-out architectures benefit from high-radix optical switches and co-packaged optics (CPO), which integrate optical transceivers directly with switch ASICs, minimizing electrical trace lengths and power consumption while achieving higher bandwidth density [88]. Modular solutions such as photonic interposers and chiplets enable flexible scaling and system-level integration.

HPC infrastructures impose stricter requirements on latency, jitter, and bandwidth uniformity, which are critical for tightly coupled applications such as AI model training and scientific simulations. Optical links in HPC commonly employ point-to-point fiber connections, optical circuit switching, and photonic backplanes. The integration of silicon photonic transceivers with compute or memory chiplets, through either 2.5D or 3D co-packaging, reduces electrical parasitics and interconnect lengths, enabling higher lane rates, improved bandwidth density, and more efficient thermal management [89] [90].

Both data center and HPC optical networks rely on modular photonic integration to accommodate scale-out and scale-up requirements. Co-packaged optics, photonic chiplets, and interposers provide standardized interfaces, enabling cost-effective assembly and improved reliability [91]. Silicon photonics, combined with advanced coupling techniques such as edge couplers ensures efficient optical I/O, supporting the growing demands of AI, HPC, and cloud computing applications [92].

Feature	Data Center	HPC
Architecture	Scale-out, large number of nodes	Scale-up, high-performance compute clusters
Interconnect Type	Ethernet, InfiniBand, DWDM	Point-to-point, optical circuit, photonic backplanes
Integration Approach	Co-packaged optics, photonic interposers	Silicon photonics, 2.5D/3D co-packaging
Performance Focus	Bandwidth per rack, energy efficiency	Latency, jitter, bandwidth uniformity
Emerging Technologies	PAM-4, DWDM, photonic chiplets	Silicon photonics, CPO, photonic interposers

Table 2: Summary of Optical Networking Approaches in Data Centers and HPC

In data center networking, pluggable optical transceivers and CPO are complementary approaches, each optimized for different deployment scenarios. Pluggables remain widely adopted due to their

flexibility, lower initial costs, and mature ecosystem, compatible with existing infrastructure, particularly in scale-out networks and non-AI workloads. Their standardized interoperability and operational simplicity make them attractive for cloud providers and enterprises that prioritize modularity and incremental upgrades. Advances in new material based optical technologies, including thin-film lithium niobate (TFLN), barium titanate (BTO), and polymer modulators, further enable pluggables to achieve low power consumption while maintaining reasonable cost. In contrast, CPO offers superior bandwidth density, power efficiency, and scalability, making it particularly suited for AI-driven scale-up networks and high-performance computing environments. However, its adoption is constrained by high manufacturing complexity, elevated costs, limited standardization, and the need to demonstrate reliable serviceability, manufacturability, and testability. As a result, pluggables are expected to persist at compute nodes and within legacy systems until CPO technologies mature and achieve broader industrial adoption.

Chapter 4 Photonics for Next Generation Computing

This chapter provides a concise introduction to application of photonic technologies for next generation computing paradigms - neuromorphic photonics, which combines brain-inspired processing with ultrafast light, photonic reservoir computing—particularly delay-based reservoirs on silicon chips— as well as quantum computing.

4.1 Neuromorphic Photonics & Reservoir Computing

Neuromorphic photonics couples brain-inspired information processing with the ultrafast, low-loss transmission properties of light. Within this field, photonic reservoir computing (RC) has emerged as one of the most experimentally mature approaches because only the linear read-out layer is trained while the internal recurrent “reservoir” remains fixed, sidestepping the need for complex on-chip learning circuitry [93].

One popular approach for neuromorphic photonics are delay-based reservoirs which have already been shown to match digital echo-state networks on benchmarks such as spoken-digit recognition and chaotic time-series prediction, while operating at multi-gigahertz rates and operating at a lower energy consumption level [94]. More recently, passive silicon photonic chips containing MZI meshes, or micro-ring arrays have pushed the concept further.

The application landscape is correspondingly broad. In fiber and free-space optical communications, photonic reservoirs already serve as adaptive equalizers that cancel chromatic dispersion and nonlinear impairments, execute packet-header recognition within tens of picoseconds, and trim bit-error rates below forward-error-correction thresholds. Radiofrequency and microwave systems employ the same hardware for real-time channel estimation and ultra-wideband spectrum classification. At the network edge, neuromorphic photonics enables sub-microsecond inference for keyword spotting, industrial anomaly detection, and biomedical sensing, where electronic latency or thermal budgets would be prohibitive. Ultrafast control loops in scientific instruments, event-driven machine-vision systems operating at tens of mega-frames per second, and physical-unclonable-function security modules have likewise emerged as fertile ground for the technology.

Several physical characteristics underpin these achievements. Photons traverse waveguides at roughly two hundred thousand kilometers per second, endowing integrated reservoirs with intrinsic bandwidths in the tens of gigahertz and, in principle, terahertz when paired with frequency-comb sources. Because passive silicon waveguides present very low propagation losses, the dominant energy cost shifts to electro-optic conversions. Parallelism scales naturally through wavelength-division and space-division multiplexing, while silicon photonics foundries facilitate co-packaging with advanced CMOS nodes. Nonlinearities—ranging from carrier-induced index changes and two-photon absorption to Kerr effects and phase-change materials—supply optical activation functions without the heavy overhead of digital circuitry.

Although researchers are exploring gated recurrent units, diffractive convolutional front ends, and graph-based spectral networks, reservoir computing remains the most practical architecture for near-term deployment. Packaging, weight precision, and standardized photonic-design toolchains still need refinement, yet the rapid convergence of frequency-comb sources, phase-change synapses, and three-dimensional electronic–photonic integration suggests that neuromorphic photonic reservoirs could graduate from laboratory curiosities to commercially deployed accelerators within the coming decade, establishing a new class of ultrafast, energy-efficient computing hardware.

4.2 Quantum Optical Computing

This chapter gives an overview of Quantum Optical Computing. The concept and basic concept of quantum computing is first introduced, followed by a section on the definition of photonic qubit encoding. The principle of linear optical quantum computing (LOQC) is described as well as a section dealing with integrated quantum photonics. The last part of the chapter touches the topic of Quantum Error Correction, presents the main quantum algorithms and the main applications.

Quantum computers use the properties of quantum systems for computation, achieving exponential speed-ups for certain tasks. A well-known example is Shor's algorithm [95], which efficiently factors large integers and thus presents a threat to many modern encryption methods. Another prominent example is Grover's algorithm [96], which provides a quadratic speed-up for search problems. Quantum computers process information using quantum bits (qubits), which can be implemented in material platforms such as trapped ions or in optical systems.

The concept of optical quantum computing dates back to 1989, when the first optical quantum gate, the Fredkin gate, was proposed [97]. However, this gate required large non-linearities which are very weak at single photon levels. In 2001 it was shown, that optical quantum computing is possible only with single-photon sources, single-photon detectors and linear optical elements [98]. This approach is known as linear optical quantum computing (LOQC). This proposed protocol, known as the KLM protocol, inspired a push towards quantum computers based on photons [99].

By employing photons as qubits, several advantages can be exploited [99] [100] [101] [102]. Photonic technologies are mature and quantum phenomena such as superposition, interference and entanglement can be generated and controlled under ambient conditions. The weak interaction of photons with the environment leads to long coherence times. Furthermore, the optical domain provides access to a broad range of degrees of freedom, including polarization, spatial and temporal modes, and frequency encoding. In addition, photonic qubits can be transmitted at the speed of light through free-space channels, optical fibers or integrated waveguides. Those advantages position photon-based quantum computers as a strong contender for the realization of large-scale quantum computers.

To realize optical quantum computing in a scalable and stable architecture, there is a growing focus on integrated photonic platforms, in which quantum circuits are miniaturized on a single chip using waveguides, beam splitters, and phase shifters [101] [103] [104]. By enabling those quantum optical computing circuits on a compact footprint, these chip-scale architectures pave the way for applications such as quantum simulation, cryptography and quantum machine learning.

4.2.1 Photonic Qubit Encodings

A qubit can be addressed as:

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$$

where α and β are complex coefficients with the normalization property $|\alpha|^2 + |\beta|^2 = 1$. The kets $|0\rangle$ and $|1\rangle$ can be written as

$$|0\rangle = \begin{pmatrix}1\\0\end{pmatrix}, \quad |1\rangle = \begin{pmatrix}0\\1\end{pmatrix}$$

in the column-vector representation. A logical dual-rail qubit can be defined using the tensor product [100] [102] [105]:

$$|\mathbf{0}\rangle = |1\rangle_{k_1} \otimes |0\rangle_{k_2} = |01\rangle$$

$$|\mathbf{1}\rangle = |0\rangle_{k_1} \otimes |1\rangle_{k_2} = |10\rangle$$

which corresponds to the dual-rail encoding of a single logical qubit in two field modes. A qubit is defined in the so-called Hilbert space $\mathbb{C}^2$ and n qubits are part of the tensorized Hilbert Space $(\mathbb{C}^2)^{\otimes n}$ [105].

Photonic qubits can be encoded by using the properties of the optical field, e.g. two orthonormal field modes. The mode pair is most commonly implemented by orthogonal polarization states

[99] $|\mathbf{0}\rangle = |H\rangle$ and $|\mathbf{1}\rangle = |V\rangle$. but other encoding schemes are also possible. Time-bin encoding represents the qubit states by photons arriving in distinct temporal intervals, and this method is robust against polarization-dependent loss in optical fibers [101] [106]. Path encoding routes photons through different optical paths to define the qubit states and this method is well suited to integrated quantum photonics [101] [107]. Spatial-mode encoding utilizes the transverse field profile of the photon which can enhance the information density [99] [108]. Additionally, frequency-mode [109] and temporal-mode [110] encodings are also attracting attention [99]. Several other qubit and qubit encodings, such as single-rail [111], parity-state [112], continuous-variable [113], and hybrid schemes [114], are also in the domain of active research [99], but a detailed description lies beyond the scope of this brief overview.

Encoding qubits in photons requires high-quality single photons. These photons must satisfy the requirements of (a) being efficiently collected into the circuit, (b) being in an indistinguishable quantum state, and (c) being compatible with detection technologies and low-loss materials [99]. However, current technologies do not fully meet all these requirements. To generate single photons single-photon sources (SPS) are employed [101] [115]. These can be deterministic or probabilistic. Deterministic SPSs, such as color centers [116] or quantum dots [117], are systems that emit exactly one single photon on demand with a high probability of success [118]. On the other hand sources such as four-wave mixing [119] or spontaneous parametric down-conversion (SPDC) [120] generate photons only with a certain probability. SPDC has become the standard workhorse of experimental quantum optics, as it can approximate the requirements above [99]. In this process, a pump photon is converted into a pair of lower-energy photons, referred to as signal and idler, while conserving momentum and energy. SPDC enables the generation of “heralded” single photons, where the detection of one photon announces the presence of its partner. Moreover, SPDC sources can directly produce entangled photon pairs in several degrees of freedom [99], including polarization [121], spatial modes [122], and frequency [123].
In order to measure the states of photonic qubits, single-photon detectors are required [101] [124]. Common implementations include avalanche photodiodes (APDs) [125], superconducting nanowire single photon detectors (SNSPD) [126] or transition-edge sensors (TES) [127]. Important characteristics of detectors are detection efficiency, dark count rate and photon-number-resolving capabilities [99]. APDs were the first devices demonstrating single-photon counting [125]. However, their relatively low detection efficiency of up to 65% [99] has motivated the adoption of SNSPDs. These operate by passing a current through a superconducting nanowire close to its critical current. Absorption of a photon induces a transition to the normal resistive state, which produces a measurable voltage pulse [99]. SNSPDs achieve detection efficiencies higher than 95% for some wavelengths [128], though they lack photon-number resolution [99]. For applications requiring photon-number-resolving detection, TESs are employed [99]. Here, photon absorption leads to a monotonic change in resistance that depends on the number of absorbed photons.

Electro-optic devices such as Pockels cells enable active polarization control by applying an external electric field [99] [129]. In addition, technologies for manipulating other photonic degrees of freedom,

including spatial [130] and frequency-time modes [131], are under development [99]. Approaches that allow conversion between different encodings, e.g. from polarization to spatial modes [132], are also being explored [99].

4.2.2 Linear Optical Quantum Computing

Linear optical quantum computing (LOQC) refers to the use of linear optical elements [102]. Typical linear optical elements are for example beamsplitters and phase shifters [100]. "Linear" indicates that these devices act linearly on the mode operators $a_k^\dagger$ and a_k which are the creation and annihilation operators respectively. A lossless beamsplitter can be described by a unitary operator [102]

$$U_{bs}(\theta, \varphi) = e^{\theta(a_1^\dagger a_2 - a_1 a_2^\dagger)}$$

and implements the rotations

$$U_{bs}(\theta, \varphi)|\mathbf{0}\rangle = \cos\theta\,|\mathbf{0}\rangle + \sin\theta|\mathbf{1}\rangle$$

$$U_{bs}(\theta, \varphi)|\mathbf{1}\rangle = \cos\theta\,|\mathbf{1}\rangle - \sin\theta|\mathbf{0}\rangle$$

A phase shifter can be described by the unitary operator

$$U_p(\delta) = e^{-i\delta(a_1^\dagger a_1 - a_2^\dagger a_2)}$$

yielding a relative phase between the two modes

$$U_p(\delta)|\mathbf{0}\rangle = e^{-i\delta}|\mathbf{0}\rangle$$

$$U_p(\delta)|\mathbf{1}\rangle = e^{+i}\ |\mathbf{1}\rangle$$

Both transformations are single qubit transformations or single qubit gates. A combination of the beamsplitter and phase-shifter can generate arbitrary single qubit states. Because they act linearly on the qubits they are classified as linear-optical gates. These quantum gates form the fundamental toolbox for manipulating photonic qubits and performing complex calculations [101] [133].

The previously described single qubit gates are easy to implement [101] [102] [134] [135]. However, two-qubit gates [136] [137] or multi-qubit gates, crucial for universal quantum computing, are much harder to implement [101]. The CNOT-gate for example is a two-qubit gate where one photon "controls" the other. Realizing such a gate requires large nonlinear interaction due to the very weak interaction between photons. However, at single photon intensities, nonlinear effects are extremely low.

To overcome this problem, Knill et al. [98] (KLM) proposed a circuit-based protocol in which the outcome of a measurement determines whether a gate has been successfully implemented. In this scheme, two-qubit gates are realized using only linear optical elements, single-photon sources, and detectors, together with post-selection [8]. Post-selection implies that the gate operation is accepted only when a heralding detector signals success. In such cases, the action of the probabilistic gate can be teleported onto the logical qubits [99] [100] [101] [102] [138]. Quantum teleportation is the transfer of an unknown qubit state onto another qubit [138] [139] and here it is used to map the successful gate operation onto the control and target qubits. Since the success probability of such non-deterministic gates is very low, additional ancilla photons and associated circuitry are required to boost the overall efficiency [99]. The KLM protocol showed that deterministic two-qubit gates are possible in principle within a linear optical framework and this has stimulated the development of

various photonic encodings, quantum gate schemes, and demonstrations of protocols and algorithms [99] [100].

However, for practical LOQC the KLM protocol is too resource-intensive [100]. An improvement of this protocol are so called cluster-state techniques or measurement based quantum computing (MBQC) [100] [138] [140] [141] [142] [143]. In the cluster-state model the computation starts with an entangled state of many qubits. This state is sent into a circuit consisting only of deterministic single-qubit operations and measurements, where each measurement basis depends on the outcomes of the previous measurements. As the computation proceeds, the entanglement is progressively consumed, and the cluster must be continually extended by adding newly generated photons. Compared with the original KLM protocol, the cluster-state model achieves a substantial reduction in resource overhead, which makes it a more practical route toward scalable optical quantum computing [99] [100] [138] [143]. Experimental proof-of-principle demonstrations of the cluster-state model have already been reported [144] [145] [146].

In the circuit-based KLM approach, the preparation of photons is easy, while the implementation of two-qubit gates is the hard part. In contrast, in measurement-based or cluster-state quantum computing creating large entangled cluster states is the hard part, whereas the computation proceeds through simple single-qubit measurements. Both models face significant overhead, either in auxiliary photons (KLM) or in the generation and maintenance of large-scale cluster states (MBQC). This trade-off has motivated the development of fusion-based quantum computation (FBQC) [105] [147]. Here, the starting point is similar to MBQC, but instead of preparing one large entangled resource state, the computation begins with small cluster states. These states are then connected through local entangling measurements, known as fusion operations, which progressively build up larger cluster states. By fusing smaller cluster states, the resource requirements are reduced compared to both KLM and conventional MBQC.

4.2.3 Integrated Quantum Photonics

Photonic integrated circuits (PICs) offer a particularly attractive platform for quantum computing. Their waveguide architecture yields high phase stability and mechanical robustness, while the technology supports the integration of essential building blocks, such as single-photon sources, beam splitters, phase shifters, and detectors on a single chip. Compact, stable, and scalable structures that are appropriate for practical quantum technologies are provided by integrated photonics, as opposed to conventional bulk optical setups, which are constrained by size, complexity, and stability concerns [101] [148] [149].

There are different material platforms used for integrated quantum photonic circuits. Due to its compatibility with mature CMOS, Silicon (Si) is widely used for fabrication, featuring precise and cost-effective large-scale manufacturing [101] [9] [150]. On the other hand, Silicon nitride applies to high-coherence quantum circuits as it provides low propagation loss and a wide transparency window [101] [151]. Additionally, for fully integrated quantum photonic systems, Indium phosphide is used as it offers the integration of active devices such as lasers and detectors [101].

A scalable quantum photonic platform needs the seamless integration of several building blocks. Single-photon sources, such as quantum dots or nonlinear processes (parametric down-conversion, four-wave mixing), for generating indistinguishable photons. For precise manipulation and unitary transformations of quantum states, several components can be used, including waveguides, beam splitters, and phase shifters etc. In terms of efficient state measurement, single-photon detectors, including superconducting nanowire detectors and avalanche photodiodes, can be used [101].

One of the most optimistic paths is the use of programmable photonic chips, which comprise reconfigurable networks of tuneable optical components like interferometers and phase shifters [152] [153]. These kinds of chips can execute a variety of quantum circuits on the same hardware, featuring flexible quantum algorithms without the need for application-specific devices. This reconfigurability shows in proof-of-concept quantum operations with high fidelity. Another key development is the integration of quantum memory [154]. Photonic qubits can be stored and retrieved in order by quantum memory devices like rare-earth-doped crystals or atomic ensembles.

Regardless of these advances, there are some challenges that remain. Due to the losses in waveguides and couplers, quantum state fidelity weakens [155]. While improvements in fabrication are necessary to control large interferometer arrays. Improvements in lithography, novel low-loss materials, and innovative design automation are key to tackling these issues. In terms of the software side, researchers can now simulate and optimize photonic circuits before implementation by using toolkits like Xanadu's [156] Strawberry Fields and IBM's Qiskit [157] [158]. Hybrid approaches that combine photonic platforms with other quantum systems, like superconducting qubits or trapped ions, are promising [159]. Photons are ideal for carrying quantum information and have long coherence time, while matter-based qubits allow strong interactions essential for computation. Therefore, Integrated quantum photonics is a keystone for scalable quantum computing.

4.2.4 Quantum Error Correction & Fault Tolerance in Photonics

Errors play a central role in quantum computing. For large-scale practical quantum computing, error correction must be implemented to achieve fault tolerance [160]. At present, quantum computers can be divided into two categories: noisy intermediate-scale quantum (NISQ) devices and fault-tolerant architectures. No fully fault-tolerant quantum computer has been realized today [161]. Existing systems fall into the NISQ category. In NISQ devices, errors occur with a certain frequency. If the error rate can be reduced below a specific threshold, quantum error-correcting can suppress these errors, enabling the transition from a NISQ device to a fault-tolerant quantum computer [161]. This principle is given by the threshold theorem [162]. For optical cluster-state quantum computing, threshold values have been investigated [138]. E.g., in ref. [163] it was shown that efficient optical quantum computing is possible when the product of detector and source efficiencies exceed 2/3. However, more complete treatments give thresholds of 10^{-3}-10^{-4} when more sources of noise are considered [164]. For FBQC, recent analyses demonstrate significantly higher thresholds, with loss tolerances of up to 10.4% per fusion operation, indicating improved fault-tolerance prospects for photonic architectures [147].

One simple illustration of error correction is the redundancy code, where more information is transmitted than the raw data itself [161] [165]. Classically, instead of sending a single bit, one could send each bit multiple times:

$$0 \rightarrow 0\,0\,0$$

$$1 \rightarrow 1\,1\,1$$

If a bit flip occurs, e.g. 0 1 0, the original value can be recovered by majority voting. In quantum systems, however, the no-cloning theorem forbids copying unknown qubits, and a majority vote would measure (and collapse) the state. A quantum analogue uses entanglement instead of copies:

$$\alpha|0\rangle + \beta|1\rangle \rightarrow \alpha|000\rangle + \beta|111\rangle$$

By measuring pairwise parities with ancillary qubits, bit flips can be identified without destroying the superposition. While this simple redundancy code serves as an introductory example, practical

quantum computing relies on stronger error correction codes. But the core idea of quantum error correction is to encode one logical qubit across many physical qubits so that errors can be detected and corrected, yielding a more robust logical state.

4.2.5 Quantum Algorithms & Application Landscape

Optical quantum computing is expected to impact a broad range of applications, and demonstrations of quantum computational advantage with photonic platforms have already been reported, e.g. in ref. [166] [167]. In the latter work, Gaussian boson sampling was implemented on a time-multiplexed, photon-number-resolving photonic processor. For this task, the best classical algorithms running on the most powerful supercomputers would require more than 9000 years to generate a single sample from the target distribution. The optical quantum computer produced a sample in just 36 µs.

One of the most important applications of quantum computing will be quantum simulation [101], which was Richard Feynman's original idea back in 1982 [168]. Since photons can exist in superpositions and entangled states, optical quantum computers can access computational regimes that are note possible for classical computers. They could be employed to model the behavior of complex molecular structures, materials and chemical reactions with high accuracy [101]. This capability will have an impact in areas such as pharmaceuticals and materials science.

Another promising application area for optical quantum computers is optimization. Grover's algorithm [96], as mentioned in the introduction, provides a quadratic speed-up for search problems. The field of quantum optimization is already beginning to show impact in domains such as route planning and logistics, with the potential to reduce transportation costs [169].

Quantum machine learning [101] [170] is an area where optical quantum computing could have a significant impact. At the heart of most machine learning algorithms lie matrix multiplications, which in principle could be performed at the speed of light within a photonic processor core [171]. By exploiting photonic qubit encodings, such systems may enable more efficient processing of large datasets compared to classical approaches. Potential applications include for example natural language processing, image recognition and large-scale optimization [101].

Cryptography is another domain in which photons and optical quantum computers play a central role [101] [172]. Quantum key distribution (QKD) enables provably secure communication, since any attempt at eavesdropping on the transmitted photons can be immediately detected. At the same time, quantum algorithms also pose risks to classical cryptography: as mentioned in the introduction, Shor's algorithm [95] threatens widely used encryption schemes by efficiently factoring large integers, which form the mathematical foundation of many current cryptographic protocols.

Chapter 5 Design, Simulation & Fabrication Workflows

This chapter gives an overview of the most popular design and simulation tools used by the photonics community, categorized depending on the solver approach, the domain where the solver works and problem solving. The final section of the chapter describes the main parameters or metrics to be considered for quantifying the performance and quality of the PICs during the test and characterization phase.

5.1 Photonic Design Automation (PDA) Tools

PDA tools form the bridge between an optical schematic and a fabrication-ready layout for PICs. Central to every PDA workflow is the GDSII file, the de-facto interchange format that foundries accept for mask writing. Designers first create the layout by placing and parameterizing waveguides, modulators, heaters, and other components within a PDA environment. Once the geometry is finalized, the tool exports a GDSII file that captures every polygon and layer with sub-micron precision. Foundries then translate these layers into physical masks, and those masks guide the lithographic steps that ultimately pattern each material layer on the wafer.

Several software platforms dominate this stage of the design flow. IPKISS from Luceda Photonics offers a Python-based, fully parametric approach tightly integrated with commercial process-design kits, enabling automated design-rule checking and direct links to optical and electrical simulations. Nazca Design, an open-source alternative, is likewise scriptable in Python, which makes it popular for rapid prototyping, hierarchical layout reuse, and straightforward version control. Cadence Virtuoso Layout Suite extends the company's well-established electronic-design environment to photonics, allowing mixed electronic and photonic design within the same database and providing mature sign-off and verification tools. Each of these platforms output standard GDSII, so a designer can move from layout to mask fabrication and thus to wafer fabrication without ambiguity, while retaining the flexibility to switch tools or foundries as project needs evolve.

5.2 Modeling Techniques (FDTD, BPM, Eigenmode, SPICE-Like)

Modeling techniques such as Finite-Difference Time-Domain, Beam Propagation Method, Eigenmode Expansion, and SPICE-like circuit simulation provide the numerical backbone of photonic design. Before a circuit reaches the layout stage, each individual building block must be analyzed to verify that it meets optical, thermal, and electrical specifications. Full-wave solvers predict how guided modes evolve, how resonators behave, and how devices interact with fabrication tolerances; the resulting scattering parameters or equivalent lumped models are then passed to layout and system-level tools so that the complete photonic integrated circuit can be optimized for performance and yield.

Finite-Difference Time-Domain (FDTD) is a time-domain, Maxwell-equation solver that advances the electromagnetic fields on a Yee grid [173]. Because it captures all wave phenomena without approximation, FDTD is regarded as the gold standard for broadband, high-accuracy analysis of nanophotonic structures, albeit at a significant computational cost. The Beam Propagation Method (BPM) solves a one-way wave equation in the frequency domain and is therefore much faster; its paraxial assumption makes it ideal for slowly varying waveguides, tapers, and fiber couplers, but less accurate for strong back-reflections or sharp discontinuities [174]. Eigenmode Expansion (EME) decomposes the cross-section of a waveguide into its supported modes and propagates their amplitudes piecewise [175]. By stitching together mode maps along the device, EME handles discontinuities more rigorously than BPM while remaining orders of magnitude faster than FDTD for long, straight components. SPICE-like approaches treat each device as a compact model described by

scattering matrices, transfer functions, or Verilog-A equations [176]. They enable rapid simulation of large-scale PICs, facilitate co-simulation with driving electronics, and support statistical analysis of process variations, although they lack the fine-grained field detail provided by full-wave solvers.

Solver	Method/Domain	Best suited for	Strengths	Example tools
FDTD	Full-wave, time domain	Nanoscale devices, resonators, broadband/transient, nonlinear effects	High fidelity, captures all wave phenomena	Ansys Lumerical FDTD, MEEP, OptiFDTD, CST
BPM (Beam Propagation Method)	Paraxial, frequency domain (one-way)	Long/adiabatic waveguides, tapers, fiber couplers	Very fast for long, slowly varying structures	RSoft BeamPROP; Lumerical MODE (BPM)
EME (Eigenmode Expansion)	Modal, piecewise propagation (frequency)	Mux/demux, mode converters, discontinuities	Much faster than FDTD for long devices, handles discontinuities well	Lumerical MODE (EME), Photon Design FIMMPROP
FEM/FDFD	Full-wave, frequency domain	Resonators, anisotropic/complex materials	High accuracy, flexible materials and boundaries	COMSOL Multiphysics, CST, HFSS
RCWA	Fourier/rigorous coupled-wave, frequency	Gratings; metasurfaces, photonic crystals	Very efficient for periodic structures	RSoft DiffractMOD, S4
Circuit/SPICE-like	Network-level scattering/compact models	Large PICs, co-sim with electronics, yield/Monte Carlo	Very fast, PDK integration, electronics co-sim	Lumerical INTERCONNECT, VPIphotonics, OptiSPICE, Caphe

Table 3: Summary of commercial solvers, the method used and their most suitable application

Sources: [177], [178], [173], [174], [175], [179], [176], [180], [181], [182], [183], [184].

Commercial software packages bring these algorithms into ready-to-use environments. Ansys Lumerical offers FDTD, MODE (which includes BPM and EME), DEVICE, and INTERCONNECT for circuit-level SPICE-like simulation. COMSOL Multiphysics provides a finite-element platform that covers frequency- and time-domain optics as well as thermo-mechanical effects. The Synopsys RSoft Photonic Suite includes FullWAVE FDTD, BeamPROP BPM, and DiffractMOD rigorous coupled-wave analysis. VPIphotonics Integrated Systems and Design Suite focuses on circuit- and system-level SPICE-like modeling with seamless links to measured or simulated S-parameters. Photon Design's FIMMWAVE and Optiwave's OptiFDTD, OptiBPM, and OptiSPICE offer additional options, while Silvaco and CST Studio also contribute specialized solvers. These tools let designers choose the most suitable algorithm for each component, strike the balance between accuracy and throughput, and feed validated models directly into the broader design, simulation, and fabrication workflow.

5.3 Test & Characterization (S-Parameters, Eye Diagrams, Q-Factor)

In the design, simulation, and fabrication workflows of photonic integrated circuits (PICs), test and characterization form the essential feedback loop that validates modeled performance against fabricated reality. While electronic integrate circuits (ICs) benefit from mature electronic design automation (EDA) flows and standardized post-fabrication testing, PICs must consider multi-physical domains (optical, electrical, and thermal) which adds more complexity to the validation process [58]. Accurate characterization becomes indispensable for establishing confidence in the predictive power of design tools, ensuring manufacturability, and enabling yield optimization in large-scale photonic foundries [185] [186].

A first level of validation typically involves frequency-domain characterization via S-parameters, which quantify transmission and reflection across a broadband spectrum. For modulators and detectors, S-parameters provide critical data on insertion loss, impedance matching, return loss, and electrical bandwidth, which can be directly benchmarked against circuit-level electromagnetic simulations [187]. The translation of these frequency-domain results into the time domain is

achieved through eye diagrams, which reveal the dynamic signal integrity under realistic modulation formats (e.g., NRZ, PAM-4). The degree of eye opening correlates with the system's tolerance to timing jitter, inter-symbol interference, and noise, thereby offering a clear link between device-level impairments and system-level bit-error rate (BER) [188] [189].

Q-factor analysis complements eye diagrams by providing a quantitative signal-to-noise metric, typically extracted from histogram fitting of logical "1" and "0" levels. This allows a direct mapping between experimental optical link performance and BER predictions, serving as a bridge between device characterization and communication system simulations [190]. Additional performance indicators, such as extinction ratio, responsivity, and modulation efficiency, further complete the validation framework, enabling the calibration of compact models used in photonic design automation (PDA) [190] [58].

The discrepancy between simulated and measured data often arises from non-idealities in fabrication, such as waveguide sidewall roughness, lithographic bias, and thermal crosstalk, that are difficult to fully capture in simulation environments. As a result, high-resolution swept-wavelength and vector network analysis techniques are increasingly employed to extract phase response, group delay, and resonance Q-factors, providing granular insight into sources of performance deviation [191]. Wafer-level test platforms now integrate optical probing, high-speed RF characterization, and automated alignment routines, enabling pre-dicing identification of Known Good Dies (KGDs) while generating large datasets for refining process design kits (PDKs) [71].

Ultimately, the role of test and characterization in PIC workflows extends beyond simple performance validation. By providing the empirical data required to calibrate design models and refine fabrication tolerances, these processes establish a virtuous cycle between design, simulation, and manufacturing. In the context of scaling photonics for data center and high-performance computing applications, such closed-loop workflows are indispensable for improving yield, reducing cost per bit, and ensuring the long-term reliability of next-generation photonic systems [192].

Chapter 6 Applications & Use Cases

In this section, we will discuss a subset of applications for photonic computing. While there are undoubtedly thousands of options and use cases for photonic systems, we will restrict ourselves to three different applications.

First, we discuss the impact of photonic computing directly on the side of calculating results in HPC workloads (specifically with an eye on AI/ML acceleration). This covers specifically the usage of photonics in traditional workloads.

Second, we will discuss the impact of photonics on communication. This – while also having obvious impact on HPC - is a broad topic that goes beyond the datacenter into wide area networks (WANs) and security in the form of Quantum Key Exchange and Quantum Key Distribution.

Finally, we will analyze the usage of photonics in sensing with a specific focus on LIDAR, where sophisticated processing in the photonic domain promises major cost savings due to the removal of expensive (and error prone) mechanical components.

7.1 AI/ML Acceleration and Data-Center Workloads

We will structure this section as follows: first we will highlight existing challenges in High Performance Computing (HPC) and current ways of solving these issues. We will then go into how and if photonics can help solve these challenges and in what ways integrating PICs may lead to further challenges in its own right.

It is important to keep these challenges and the challenges of scaling in mind due to what is commonly known as “the bitter lesson” [193] of AI: “The biggest lesson that can be read from 70 years of AI research is that general methods that leverage computation are ultimately the most effective, and by a large margin.”, this dually means that to keep up with AI/ML workloads, one has to be able to scale the compute fabric – such as photonic computing – to match the increase in “intelligence” of AI systems.

Modern AI/ML a well as HPC workloads are dominated by 3 large scaling limitations:

First, of course, is the computation itself, i.e. “given a set of inputs, produce the set of outputs”. Here we need to contrast Datacenter workloads with AI/ML and HPC workloads. The former comprises challenges such as webhosting and database access, while the latter are simulation, inference and training loads. Of course, there is some overlap – e.g. a website that hosts an LLM chatbot – but it nevertheless makes sense to contrast these due to their fundamental differences in workloads. Specifically, HPC workloads are dominated by simple “static” operations repeated at large scale, e.g. matrix-vector products that are executed at phenomenally large scales. Traditional webhosting tends to be dominated by database access, server-side HTML rendering, and similar “dynamic” operations with complex control flows. Photonic computing has the chance to excel at the former, while the latter is intractable in the near future. Current solutions mostly rely on custom ASIC components, such as NVidia's “TensorCores” to accelerate the hot, e.g. matrix-vector product, paths with a trend towards chiplet designs to easily combine different manufacturing nodes and improve both thermal management and production yields.

The second big challenge is memory management, specifically “how can data be moved from memory (e.g. DRAM) dies into the core for further processing”. Especially training loads for large transformers are nowadays dominated by memory bandwidth, which has led to a transition from traditional CPU+DRAM technologies (64 bit width, 8-n prefetch) first into GDDR (32 bit width, 16-n or

32-n prefetch) and now into HBM (128 bit width, 8-n prefetch multiplied by up to 8 stacked dice) [194]. Recent trends in HPC favor massive parallel loads and stores, which has defined the design of HBM: HBM is comparatively slow per pin but has many of them yielding thousands of bits wide data access. This increase in bandwidth has necessitated extreme designs for memory controllers and chip-internal routing to handle the amount of bit/s. Training of neural networks is mostly dominated by memory access with about 37% of wall-clock time being spent in memory bound operations [195]. This is why large-scale training is nowadays done using custom compute kernels which minimize data movement (see, e.g. [196]). Memory interactions are one of the big challenges for photonic systems since there is no such thing as a "Photonic DRAM" yet that can provide a large amount of memory. This is why systems generally store their information in existing electrical memory and move it from/to the photonic system via lasers and ADC/DAC conversion. In fact, getting information from memory into the photonic system might be one of the most significant bottlenecks depending on the design. Even though photonic systems may not facilitate memory themselves, bundling multiple operations into a photonic compute "kernel" may still help reduce overall memory pressure as data must be read and written less often.

Finally, we have communication, both chip-to-chip and system-to-system. The former refers to electrical connections across e.g. CPU cores or chiplets on the same substrate, while the latter connects independent systems with each other. While we are not aware of any Chip-to-Chip communication system – presumably due to the ADC/DAC overhead - System-to-System communication is already dominated by fiberoptic connections. The importance of communication cannot be understated: All HPC workloads rely on both per-node compute scaling and scale-out across as many nodes as possible, which not only allows for higher total throughput, but also allows for more efficient usage through, for instance, "Composable Infrastructure". In HPCs and datacenters designed around Composable Infrastructure, any system resource like compute, storage, RAM, etc., is put into a "pool" which is flexibly assigned to "virtual nodes" allowing for flexible combinations of resources. This, of course, increases the need for high bandwidth, low latency connections above and beyond what is typically possible via copper wires. Since this is a big topic even outside HPC we will move discussion of this into its own section.

The selection of limitations here shouldn't be too surprising as they are what govern most HPC workloads regardless of whether they might be - simulation, machine learning, or Genomics. The major difference between different HPC workloads is which factor dominates the overall cost of obtaining the result (e.g. in Genomics memory access is a major bottleneck).

As we moved communication into its own section below, our focus here will be a discussion of the compute itself.

On the compute level, PICs can already be used to accelerate tiny neural networks (in the order of dozens of neurons). Generally, there are two ways of scaling this to larger models: First, one can aim for accelerating the entire NN from input to output in a single "photonic block". This necessitates the implementation of a wide variety of nonlinearities, normalizations, and of course matrix-vector multiplications inside the photonic domain. This offers the highest total acceleration due to the lack of ADC/DAC conversion and the total removal of memory access aside from the initial "load" of the data into the system and "store" out of it [1]. This reduction in memory load in turn reduces the complexity needed for memory controllers, assuming no intermediate states are needed. However,

[1] This assumes that information is put into the system electrically. If one already has photonic data, e.g. processing of raw fiberoptic signals, then no ADC/DAC is necessary at all.

it comes with the added complexity of needing to implement a significant number of primitives and gradient computation [2].

A further advantage of keeping everything in the photonic domain is that the natural multiplexing of e.g. different frequencies, phases, or polarizations allow for batch inference over a fixed neural network.

There is also the option foregoing traditional NN designs and implementing primitives that are specifically aligned to optical computing, e.g. high resolution digital micro mirroring devices [197] which have the advantage of being well aligned with the photonic medium but force a complete restart of ML architecture search with no guarantee that high performance architectures even exist in this medium.

Aside from directly accelerating the entire neural network end-to-end, one can also imagine only accelerating the matrix-vector products and doing all (or at least many) nonlinear operations digitally. This has the appealing property that it retains almost all the acceleration benefits, while retaining a lot of flexibility and keeping the PIC design simple. Recent work profiling LLM performance reveals that 99.8% of total flops are spent on matrix multiplication [195] while the remaining 0.2% are spent on statistical norms and activation functions. This means that accelerating matrix multiplication is for all extents and purposes equivalent to accelerating NNs as a whole.

Another quite appealing property of neural network acceleration is that one can usually reduce the floating-point precision quite dramatically with negligible effect on the final output. In fact, recent works, such as DeepSeek V3 [196] compute all matrix-vector products in 8-bit floating points while accumulating weight updates in 16-bit floating points, which more than doubles the performance of contemporary accelerators. For inference, dynamic quantization techniques can reach effective compression rates of 1.8bit/weight while still keeping the network usable [198] (do note that below 4bit/weight one can expect significant accuracy loss). This reduced accuracy can allow for a certain amount of “wiggle room” when constructing matrix multiplication circuits on PICs that would not necessarily translate well to full network acceleration.

On the other hand, if one could compute high precision matrix-vector products, the resulting accelerator would also be appealing for other HPC use cases, such as simulation.

Gradient passes would also be computable “for free” since the nonlinearities are done electrically (easy gradients) and the derivatives of a matrix-vector product is trivial.

The major downside with executing only the matrix multiplication in PICs is the need for more sophisticated memory management and repeated DAC/ADC conversion. However, optical matrix multiplication should be seen as the “low hanging fruit” with a lot of academic work already done but commercialization being low (major players here are Lightmatter and Q.ANT which have commercial prototypes).

Another important consideration is the way one can implement matrix multiplication in PICs: Currently, methods can be split into two broad categories.

[2] In fact, gradient computation might be a significant bottleneck: Typically, NNs cache certain information during the forward pass to enable a faster gradient “backward” pass. This storing of information is significantly more challenging in PICs than it is in electrical systems. If the information cannot be stored, then it has to be recomputed, which slows down the system.

First, coherent implementations use coherent light sources and operations to directly implement complex-valued matrix multiplication. Coherent light has higher constraints as the phase relationships must be maintained over time and space. This means that manufacturing has harder constraints as stable narrow-linewidth sources (e.g. on-chip lasers or external coupling) must be used. Further, coherent optical circuits are more prone to path length changes (thermal drift, vibrations). However, coherent optics allows for more sophisticated encoding as interference and phase-sensitive operations are only usable if the phase is controlled in the first place. Since information can be encoded into both amplitude and phase, one can implement complex valued operations and multiplex along wavelengths, spatial modes, polarization and phases. Arithmetic can be implemented via interferometry, phase shifting, Mach-Zehnder meshes or micro-ring resonator arrays.

Second, incoherent optics rely on just intensity for information transmission and processing. This means one has a significantly lower barrier to entry: Broadband sources such as LEDs can be used as light sources and the circuits are much more tolerant against alignment errors and temperature variation as phase drift does not affect the computation. Simpler integration also means that systems can easily scale to larger problems compared to coherent systems, as the likelihood of producing a fully coherent chip reduces with the number of components used, while the robustness of coherent optics allows for significantly larger scales.

This increase in simplicity comes at a cost: One cannot naively implement complex valued matrix multiplication (or in fact “non positive” matrices) or nonlinear optics in incoherent optics. This means that one needs to (implicitly or explicitly) decompose matrices to run them in a coherent setting.

A great discussion of different implementation types (especially coherent ones) can be found in [199]. Another recent work to note is [200] which uses incoherent optics to scale matrix-vector products orders of magnitude larger than existing methods by exploiting time multiplexing.

Metric	Coherent Light	Incoherent Light
Throughput	Very high: parallel interferometric meshes can perform N×N matrix multiplications in O(1) time (optical propagation)	Moderate: limited by detector bandwidth and modulator speed (tens of GHz)
Energy Efficiency	Potentially < pJ per operation (no resistive heating), though stabilization and phase tuning add overhead	Typically, higher energy per bit (LED drive, photodetector bias) but simpler overall
Noise Sensitivity	Phase noise, coherent crosstalk, back-reflections critically affect SNR	Shot noise and thermal noise only; no phase-related noise
Scalability	Challenging: large interferometer meshes grow quadratically in components; alignment complexity scales poorly	Easier modular scaling: add more LED/detector channels linearly

Table 4: KPI comparison between coherent and incoherent light based solutions

Ultimately, coherent optics promises higher performance in the long-term (e.g. effective O(1) matrix multiplication), while incoherent options have the advantage of already scaling to real world relevant systems: For instance the system proposed by [200] promises 110 trillion multiply-

accumulate operations per second, which is close to an Nvidia RTX 490 GPU (approximately 165 trillion FLOPs) while consuming drastically less power.

The general decision between coherent and incoherent designs also comes down to whether other operations should be performed jointly: If one wants to compute nonlinear effects on the PIC (for instance for a fully optical NN) coherent optics become more important. However, if one wants to take advantage of existing manufacturing processes or needs to go back to electrical systems anyways, incoherent matrix multiplication becomes interesting. Especially time multiplexing to simulate large matrix multiplications is easier in incoherent optics due to the ability to use electrical accumulation on the detector, rather than having to use finely controlled delay lines.

7.2 Telecom and Datacom Transport

Optical interconnects are already the majority of high-throughput, low-latency communications systems. This is due to several reasons: Optical interconnects can carry dozens of wavelengths increasing throughput into the terabits/s. Further, due to the low interactions of photons with their carrying medium, single mode fibers have low attenuation in the orders of 0.2-0.3db/km allowing for longer reach without repeaters. Another point to mention is electrical isolation as no RF signals can propagate through fibers, which reduces overall noise in e.g. dense server racks. Finally, optical systems tend to use lower power than electrical ones, mostly due to the aforementioned lower resistance.

A major limitation is deployment cost: Both the installation and production of the ultrafine glass fibers and the need for fiber amplifiers or dispersion compensators make fiber impractical for short-haul deployments [201]. Reducing fiber and transceiver costs, as well as increasing sustainability, have been recent drivers of development [202] [203].

In general, much research is put into fiber technology to reduce latency- (Hollow-Core Fiber reaches the speed of light in air, rather than in glass [204]) and throughput (space division multiplexing in multicore-few mode fibers [205]).

Further, while optical networks have comparatively low power/bit, the total power necessary is still high – on the order of a couple of Watt/channel [206]. This makes usage in Hyperscalers which may have tens of thousands of connections difficult. Recent trends in optical networks reflect this: Co-packaged optics and PICs in general which integrate lasers, modulators, and detectors alongside switching ASICs offer not only higher throughput, but also lower power consumption [204].

Significant effort is also going into increasing the robustness of optical systems by deploying AI/ML methods for problems such as dynamic impairment compensation in coherent receivers, traffic prediction and bandwidth allocation in reconfigurable networks, and predictive maintenance of installed fibers/amplifiers [207]. One can easily see networking specific AI/ML models being directly deployed in the optical domain, which completely removes the conversion overhead from analog optical to digital electronic signals.

A side note we want to mention here are free-space optical systems used mostly in inter-satellite and satellite-to-ground communications [208] these systems use the fact that space has straight connection paths and a naturally near-ideal vacuum for optical communications to improve upon the traditional electric communication. Recent NASA experiments have already demonstrated 200Gb/s satellite-to-ground communications [209].

Terrestrial deployments also are being experimented with, but the lack of clear paths and e.g. weather obstructions make terrestrial free-space optics challenging [208].

Aside from Communication itself, optical methods can also lead to improved security due to the fundamental properties of optics.

Due to the low attenuation of optical systems, it is relatively easy to detect fiber tapping due to the introduction of high losses and reflections during readout (e.g. Optical time-domain reflectometer, OTDR). Recent works use imperfections in fiber (specifically their Rayleigh back-scatter patterns) to build unclonable fingerprints for device authentication [210].

This can be further enhanced via the usage of Quantum Dynamics. Specifically, Quantum Key Exchange (QKE) and Quantum Key Distribution (QKD) are realistically only possible in optical media due to the lack of a need cryogenic temperature or mTorr level vacuums.

Quantum states of light (i.e. individual photons) cannot be copied perfectly via the “No-cloning” theorem of quantum dynamics. This means that any eavesdropping measurement is forced to perturb the channel, which introduces measurable errors. The important point of Quantum based security is that the overall noise of the system must be low enough, such that an attacker can be easily distinguished from a normal error.

Broadly speaking, there are two types of Quantum security implementations: First, in “Prepare-and-Measure” (see BB84, B92 protocols) user “A” encodes bits in non-orthogonal photon states (polarization, phase, etc.) and “B” measures randomly. Mismatches in the alignment showcase eavesdropping.

Second, “Entanglement Based” methods (e.g. the E91 protocol) incorporate entangled photons shared between “A” and “B”. A simple bell-inequality test can detect intrusion into communication.

Beyond that, many more advanced methods such as “Decoy-State QKD”, “Continuous Variable QKD”, and “High-Dimensional QKD” exist to further enhance the exchanges. Specifically, the latter two methods are interesting, as they allow for the usage of e.g. commercial fiber (in the case of CV QKD, [211]) to reach ~50km in range. Further, free-space systems for Satellites have also been demonstrated. Standardization of QKD schemes is in progress (https://www.itu.int/rec/T-REC-Y.3800/).

Aside from key distribution, there are also schemes to hide the communication of users behind intrinsic quantum noise, making communication indistinguishable from noise for an outside observer [212].

7.3 Sensing, LIDAR, and Imaging

LiDAR is a powerful optical 3d scanning technique offering higher quality and performance than conventional radar at the cost of higher complexity. The major limitation of LiDAR is the high cost, driven by the need for high performance eye-safe laser or Single-photon avalanche diodes, high alignment precision of mechanical scanning assemblies and the need for high-speed electronics/ASICS to digitize the high data throughput of LiDAR systems [213].

However, this is expected to change as many of the costs such as low-volume diode production or ASIC design can be amortized as production volume increases. Further, recent technical advancements driven by the need of scalable LiDAR production in the automotive industry have further dropped costs considerably:

A recent shift is the move to solid-state architectures such as MEMS-based scanning, optical phased arrays (OPA) or flash LiDAR that allow the elimination of expensive mechanical systems [214].

Specifically interesting for photonics research, companies like Continental and DENSO have moved towards wafer-level packaging and CMOS-compatible photonics. Experts expect this trend to continue with specific focus on integrated photonics “LiDAR-on-chip” [215], large-scale OPAs [216], wide-angle no-scanning “Flash LiDAR” [217], and AI-driven signal processing for improved denoising. Specifically, on the software side there is still significant improvements to be had: Recent AI-driven approaches almost double the resolution of LiDAR with 32-beam units matching or exceeding 64-beam units just through improved AI-driven LiDAR processing [214].

Beyond those, techniques like Coherent Frequency Modulated Continuous Wave LiDAR (“FMCW (coherent) LiDAR”) [218] increase the capabilities of LiDAR towards velocity measurement and extended range, while improving interference rejection, at the cost of needing a fully coherent pipeline and increasing signal processing complexity.

There are still numerous technical challenges that need to be addressed before LiDAR can reach its full potential. Current silicon OPA have a narrow steering angle of only ~20° and suffer from large side lobes which increase the needed power and in turn require low-loss waveguides to handle the higher laser power. Managing the beam divergence, phase noise, and thermal drift remains challenging [216].

Photon efficiency is still low, especially in noise environments (daylight, rain, dust) where detectors with µW-level noise equivalent power (NEP) and complex background suppression are necessary.

On the processing side, next-gen LiDARs are expected to produce tens of gigabit per second of raw point-cloud data requiring low-power, high-throughput SLAM and object detection pipelines capable of running on automotive grade ASICS [219].

Beyond that, the laser itself can be swapped from a 905nm to a 1550nm laser for higher pulse intensity while still being eye safe. However, the lasers and related components are costlier than the more established 905nm ones. In general, alternative laser wavelengths such as 1550nm offer huge improvements in performance due to better atmospheric transmission and higher eye-safety thresholds (1550nm are expected to achieve useable 1km detection ranges, [214]).

Software is also lagging behind hardware: Specifically existing SLAM methods often buckle under higher channel counts, as the increase in resolution cannot be processed sufficiently quickly. Further, current SLAM systems often assume a dearth of usable data, rather than an excess of it.

Nevertheless, experts expect the price of high-grade LiDAR to drop from the current ~500$/unit to less than 200$ by 2030 while increasing the capabilities substantially [220].

Chapter 7 Roadmaps, Challenges & Future Directions

This chapter gives an overview of the emerging materials which can be used for the next generation photonic components, describing the most relevant aspects to be considered for heterogeneous integration of PIC, EIC and other components of the package. Software-Defined and Programmable Photonics devices are introduced as well, presenting the most relevant players on the market developing such devices and mentioning the employed technology. The last part of the chapter deals with the standardization aspects and finally closes the chapter into a section on the photonic computing related activities whiting the Fraunhofer context.

7.1 Emerging Materials (2D Materials, Phase-Change, Plasmonics, Magneto-optical Materials)

PCMs, phase change materials allow nonvolatile light modulation required for optical neuromorphic computing/optical synapses by creating the opportunity to produce reconfigurable optical networks. They are based on reversible switching between amorphous and crystalline states, that allows optical phase and amplitude modulation [221]. Further benefits are also small form factors, large optical index modulation leading to low energy consumption, and no static power. Such materials can be chalcogenide based like tellurides, selenides, and sulfides [222] [223] [224].

Another group of materials that allow nonvolatile switching are ferroelectric materials. Recent experiments employed ferroelectric hafnium zirconium oxide as a non-volatile photonic phase shifter [225]. Its main appeal is its CMOS-compatibility, which makes it especially interesting for integrated neuromorphic photonics. Another more established ferroelectric material is BTO ($BaTiO_3$). However, BTO suffers from lattice mismatch with silicon, which requires its growth in a separate substrate, complicating the production, cost and reducing its CMOS-compatibility.

Two-dimensional (2D) materials such as graphene and transition-metal dichalcogenides (TMDs) have promising features for integrated photonic quantum and neuromorphic computing. They exhibit strong light-matter interactions, ultrafast carrier dynamics, and tunable bandgaps, supporting on-chip single-photon sources, reconfigurable modulators, and low-energy synaptic elements within a sub-micron footprint. Despite their compelling optoelectronic properties, 2D materials still sit at the margins of the semiconductor value chain, and their path to CMOS-compatible photonic quantum and neuromorphic hardware is far from assured. Reliable wafer-scale fabrication like CVD growth remains difficult, and their engineering is still challenging. PDKs and models are underdeveloped, hindering CMOS design and co-simulation, and qualification and long-term reliability data are limited, complicating standardization and supply-chain risk.

In addition to PCMs and 2D materials, plasmonic materials are being actively explored as candidates for ultrafast, deeply sub-wavelength optical computing. By confining light into nanometer-scale volumes, plasmonic waveguides and resonators can enable compact modulators, switches, and logic gates that outperform dielectric devices in terms of footprint and bandwidth. Their main advantage lies in the ability to couple photonic and electronic functionalities at unprecedented scales, which is particularly attractive for neuromorphic accelerators requiring high fan-in/fan-out connectivity. However, plasmonic devices face intrinsic ohmic losses that limit propagation length and energy efficiency. Emerging approaches such as transparent conducting oxides (TCOs), nitrides, and alternative plasmonic materials (e.g., titanium nitride, aluminum-doped zinc oxide) aim to mitigate losses while maintaining CMOS compatibility. Still, wafer-level integration, reproducibility, and

thermal stability remain open challenges before plasmonic elements can be adopted in mainstream silicon photonics PDKs.

Magneto-optical (MO) materials represent another frontier, enabling nonreciprocal light propagation, isolators, and reconfigurable memories in photonic circuits. Garnet-based MO films (e.g., yttrium iron garnet, YIG) have long demonstrated strong Faraday rotation, but their growth on silicon is not trivial due to lattice mismatch and the need for epitaxial quality. Recent progress in sputtered or hybrid-integrated garnets, as well as all-optical control of spin states in 2D magnets and ferrimagnets, suggests possible paths toward CMOS-compatible MO devices. For optical neuromorphic computing, MO materials are attractive because they offer nonvolatile state retention (spin order) and can serve as reconfigurable weight elements in photonic neural networks. Yet, their integration density, compatibility with high-volume CMOS fabs, and long-term stability under repeated optical cycling remain critical gaps.

Taken together, emerging materials for optical computing each bring distinct trade-offs:

- PCMs → mature nonvolatile switching, small footprint, low energy; good pathway toward silicon co-integration
- Ferroelectrics -> good pathway toward silicon co-integration (especially HfO_2/ZrO_2 systems).
- 2D materials → unmatched tunability and multifunctionality, but lack scalable, defect-free, CMOS-grade fabrication.
- Plasmonics → extreme confinement and bandwidth, but energy efficiency limited by losses.
- Magneto-optical materials → enable nonreciprocal and nonvolatile functionalities, but integration and CMOS compatibility remain immature.

A unifying challenge across all platforms is the translation of laboratory-scale demonstrations into CMOS-foundry-compatible, wafer-scale, and reliable processes. The eventual success of optical neuromorphic and quantum hardware may hinge on heterogeneous integration: combining PCMs for memory, 2D materials for tunability, plasmonics for density, and MO materials for nonreciprocity, within the reliability envelope of silicon photonics.

7.2 Heterogeneous & 3-D Integration (Electronics + Photonics + MEMS)

As mentioned previously in chapter 3, packaging for PICs is the discipline of co-integrating optical, electrical, and thermal subsystems into a manufacturable module that preserves link budget, signal integrity, and reliability from wafer probe to field deployment. Compared to electronic ICs, PIC packaging must simultaneously route high-frequency (HF) electrical signals and low-loss optical I/O with micron-scale alignment tolerances, while managing thermo-mechanical stresses across dissimilar materials and keeping parasitic and reflections within tight budgets. As a result, packaging and testing often dominates module cost and time-to-yield in photonics, and requires co-design across optics, RF, and mechanics rather than a purely sequential flow [226] [227] [228].

The following packaging related aspects are the most relevant to be taken into account:

- High-frequency signal integrity (SI). The HF paths—from drivers/TIAs to on-chip modulators and photodiodes—are engineered as impedance-controlled transmission lines (e.g., CPW or microstrip) across PIC pads, interposer, and PCB. Wire-bond length, bump geometry, and return path continuity determine insertion loss, return loss, crosstalk, and jitter. Accurate EM co-simulation across die, interposer, and package (including via fields and connectors) is

essential to maintain target S-parameters over tens of gigahertz; design rules typically limit bond lengths and enforce 50-Ω (or differential) references across discontinuities [226] [227] [229].

- Power integrity (PI). Co-packaged drivers/TIAs and control ASICs impose stringent supply impedance targets to suppress supply-induced jitter and thermal noise in analog front-ends. Decoupling networks and low-ESL capacitors are placed as close as possible to the die, with current-return planning and segmented power planes on the interposer/PCB to limit droop and ground bounce during bursty traffic typical of datacom/HPC workloads [226] [227] [229].
- Optical connectivity. The package must provide mechanically stable, low-loss coupling between on-chip waveguides and external media (SMF, MCF, or fiber arrays). Common strategies include edge couplers with spot-size converters, vertical grating couplers for wafer-level test and array attach, and evanescent/photonic-wire-bond interfaces for heterogeneous die-to-die links. Each option trades bandwidth, polarization dependence, alignment tolerance, and manufacturability; array attach and active/passive alignment choice strongly influence cycle time and yield [227] [228] [230] [231].
- Thermo-mechanical design and thermal management. Photonic devices (e.g., lasers, resonators, phase shifters) are sensitive to temperature and stress; coefficient-of-thermal-expansion (CTE) mismatches across Kovar/ceramic/Si/organics can induce phase drift, birefringence changes, and coupling loss. Packages therefore integrate heat spreaders, TECs/NTCs, and low-θJA paths from hotspots (drivers, lasers) to the ambient, while mechanical fixtures (stiffeners, underfill) mitigate warpage and vibration. Multi-physics co-simulation (FEA + CFD) is standard to predict thermal gradients, stress fields, and their impact on optical phase and alignment stability [226] [227] [228].
- Manufacturability, test, and reliability hooks. To achieve KGD yield, layouts include dedicated probeable optical/electrical ports, keep-out zones for fiber arrays/RF probes, and alignment fiducials for automated active/passive attach. Wafer-level optical probing via grating couplers reduces screening cost; reflective probe schemes extend wafer-level test to edge-coupled designs. Design-for-reliability (DfR) adds hermeticity, contamination control (flux/solvent management near optics), and re-workability where feasible. Long-term reliability is verified by Telcordia/IEC stress (HTOL, THB, temp cycling, vibration) with photonic-specific monitors (IL/PDL drift, resonator detuning, RIN penalty), and by correlating SI/PI/thermal margins to BER/eye metrics under stress [226] [227] [228] [232] [233].

Nowadays for high performances applications optical engines have to be co-located with switch/compute ASICs to shorten electrical reach and reduce energy/bit, this is called co-packaged optics (CPO). Two packaging vectors are prevalent: (i) 2.5D integration on Si/organic interposers for routing density and manufacturability; (ii) 3D stacking with TSVs or silicon bridges for higher beachfront (Tb/s/mm) and lower parasitics - at the expense of thermal density and assembly complexity. Photonic wire bonding and photonic interposers further decouple optical I/O placement from ASIC edges, improving bandwidth density while imposing new alignment and process controls [229] [230] [231].

The package form factors depend on the application, and it is a trade-off in performance and miniaturization of the component. The following form-factors can be mentioned: hermetic “gold-box”/butterfly-style modules (Kovar/ceramic feedthroughs) for more environmental control; PIC-on-board test vehicles and evaluation boards for rapid characterization; pluggable transceivers (e.g., QSFP-DD/OSFP) where modularity and serviceability are more relevant; CPO for scale-up AI/HPC

fabrics; and specialized assemblies such as photonic chiplets on Si/glass interposers and photonic-wire-bonded multi-die systems for heterogeneous integration [227] [229] [230] [231].

Fiber Optic Assembly (Pigtailing)

Active alignment remains one of the dominant approaches for ensuring efficient optical coupling in photonic integrated circuits (PICs), particularly in high-performance modules. Unlike passive alignment, which relies on lithographic precision and mechanical tolerances, active alignment exploits real-time optical feedback to optimize fiber-to-chip or device-to-device coupling efficiency. While this technique enables high coupling performance, it continues to face limitations in terms of scalability, throughput, and cost, which pose challenges for volume manufacturing [234] [235].

The process typically begins by injecting optical power either from an external laser source, coupled through a fiber patch cord, or by activating integrated light sources such as lasers or modulators on the PIC itself [236]. Optical signals are then monitored at designated output ports, where detection can be performed either via external photodetectors or via photocurrent from integrated photodiodes. Once initial light is detected, closed-loop optimization algorithms—commonly based on gradient ascent or "hill-climbing" routines—are applied to iteratively adjust the fiber or device position until maximum transmission is reached [237].

At the point of optimal alignment, the coupling interface is fixed by means of mechanical or adhesive stabilization techniques such as UV-curable epoxies, solder bonding, or localized laser welding. These approaches secure sub-micron stability of the aligned components while maintaining acceptable optical insertion loss [238]. However, the curing or welding step can introduce thermal stress or long-term reliability concerns, particularly in high-power or temperature-varying environments, which underscores the importance of careful packaging design [186].

For PICs with multiple optical input/output (I/O) channels, alignment complexity scales rapidly. To mitigate this, integrated optical shunt structures (or optical loops) are often employed. These allow alignment to be performed using only two reference fibers for light injection and collection, while the remaining fibers in a v-groove array can be aligned passively due to their precisely defined relative positioning. This hybrid approach—active alignment using reference channels combined with passive positioning of the fiber array—strikes a balance between coupling efficiency and assembly scalability [239].

Despite these advances, the intrinsic serial nature of active alignment remains a bottleneck. Emerging alternatives, such as passive alignment with lithographically defined mode converters, photonic wire bonding, or self-aligned nano-imprint techniques, are being explored to overcome throughput constraints. Nonetheless, active alignment remains a critical process in applications requiring ultra-low coupling losses, such as coherent transceivers, LiDAR, and quantum photonic systems [229] [240].

Nowadays, Fiber-to-PIC assembly relies mostly on active alignment using a high-precision 6-axis positioning system, monitoring coupled optical power to reach the optimal alignment, which is then permanently fixed via UV-curing adhesives or laser welding [241].

Several assembly approaches are commonly used:

- Lensed fiber coupling (edge coupling): Used when the PIC mode size does not match a standard single mode fiber (e.g., InP PICs). Lensed fibers—produced by laser machining, chemical etching, thermal tapering, or graded-index rods—enable mode matching, achieving typical coupling losses ~1 dB over hundreds of nm bandwidth [242].

- Butt coupling to cleaved fibers: Applied when mode matching is naturally achieved, e.g., vertical grating couplers (VGCs) in Silicon Photonics or wide-spot-size edge couplers (glass, $LiNbO_3$, thick SOI). Fiber arrays allow simultaneous multi-fiber alignment, with coupling losses as low as 1 dB and lateral tolerance ±2 µm [243] [243].
- Lens coupling: Uses optical magnification systems (single or dual lenses) to match PIC output to fiber modes. Dual-lens systems also accommodate optical isolators. Coupling losses of ~1.7 dB with alignment tolerance ±30 µm have been demonstrated for VGC arrays [244].
- Waveguide interposer coupling: Involves an intermediate waveguide (e.g., glass, polymer) between the PIC and fibers, often serving as a spot-size converter. Active alignment with UV adhesive is standard. Si–SiN–glass three-stage couplers have achieved <1.9 dB losses and low polarization-dependent loss (<0.4 dB) over >100 nm bandwidth [245].

7.3 Software-Defined & Programmable Photonics

The rapid development of data-driven technology, such as AI, 6G networks, and quantum communication, requires the fastest and most energy-efficient systems. Beyond electronics, photonics offers a promising solution to this need by using light instead of current, which is faster. However, traditional photonics devices are designed for a fixed and particular task that introduces limitations of flexibility and reconfigurability [246].

To deal with this boundary, a new concept emerged: Software-Defined and Programmable Photonics. This concept allows for control, reprogramming the function of a photonics circuit after fabrication for different tasks by using software. A single photonic chip can be used for versatile tasks like field-programmable gate arrays (FPGAs) in electronics [247].

Software-Defined & Programmable Photonics depends on different technologies that allow the real-time control of light on a PIC. These technologies facilitate performing different optical functions such as filtering, switching, modulation, and signal processing, to specify or alter them through software rather than fixing them permanently during chip fabrication [248]. Core technologies are:

- Phase shifters: control the phase of light signals through altering the refractive index of the waveguide through thermo-optic (heating) or electro-optic (voltage-driven) effects [249].
- Mach–Zehnder interferometers (MZIs): MZIs are fundamental tunable building blocks that are used for splitting and combining light. By setting the phase shifter in one arm, these components can act as switches, filters, or modulators -depending on the control signal [250].
- Waveguide Meshes: create many pathways for light to travel through a chip. Each node of the mesh can be tuned for the desired routing and transformation of optical signals across the chip [246].
- Tunable Optical Components: these components, such as variable attenuators, tunable couplers, and filters, etc. can be tuned in real-time by using electrical or thermal input.
- Control Electronics & Software Interfaces: programmable photonics are managed by integrated control electronics that interact with digital to analogue converters (DACs), drivers, and a feedback system. User's commands on high-level software tools are translated to low-level control signals by using a photonic compiler.
- Material Platform: due to compatibility with CMOS technology, Silicon is widely used for integrated photonic technology. However, other materials, in particular thin-film lithium niobate, indium phosphide, and phase-change materials, are being studied to boost speed, non-volatility, or power efficiency [246].

Several strategies and architectural approaches are used in programmable photonics. These approaches vary in how light is controlled, how the system is reprogrammed, what functionality is targeted, etc. Below are the two major approaches used in current programmable photonic platforms:

- Waveguide Mesh-Based Architectures: It is one of the most common approaches in programmable photonics, constructed upon 2d mesh networks of MZI and Phase shifters [246] [251]. The meshes can be several structures, like triangular, square, and hexagonal topologies [246]. An arbitrary linear transformation can be achieved on the light signal by altering the phase at each node. The waveguide mesh-based architectures can be used for signal processing, unitary matrix operations, optical switching, etc.
- Hybrid Material-Based Approaches: A new approach to increase tuning efficiency, speed, or introduce new functionality by combining silicon photonics with other materials. In particular, Phase-Change Materials (PCMs) have non-volatile, ultrafast optical switching competencies [246] [252]. Whether Thin-Film Lithium Niobate (TFLN) provides very low-loss and high electro-optical properties, that's crucial for high-performance modulation applications. Indium Phosphide (InP) has good performance for communication and sensing as it's excellent for active components like lasers, amplifiers, and detectors. However, Silicon Nitride (SiNx) possesses a large spectral range and ultra-low losses, making it optimal for detectors, spectrometers, and quantum computing applications.

There are additional use cases for software defined photonics beyond rapid prototyping:

- Field-Programmable Photonic Arrays (FPPAs): The FPPAs concept mimics the Field-Programmable Gate Array (FPGA) model for electronics. It allows programming of photonic circuits after fabrication by setting the configuration of basic units, such as MZIs and couplers, via software [246] [253]. This facilitates reusability and accelerated prototyping and dynamic computation on a hardware level. FPPAs can be used for optical signal processing, Photonics computing, and optical communication, etc. These naturally fit into the role FPGAs play in electronics and can be easily implemented using waveguide meshes.
- Software-Defined Optical Interconnects: A software-controlled approach that focuses on chip-to-chip data link using tunable lasers and modulators, facilitating low-latency, high-speed communication in AI devices and data centers [254].
- Neuromorphic Photonics: This concept mimics the human brain neural network by using a photonics circuit. By using tunable phase shifters or attenuators, programmable weights can be encoded, and the mesh structure performs matrix multiplication, which is the main operation of AI models [255].
- Quantum Programmable Photonics: A Quantum photonics chip based on programmable interferometers and photon sources to deploy quantum gates, entangled photon generation, and boson sampling. To perform different quantum operations, reconfigurability is very important in this type of system [256] [257].

Numerous startups, research institutes and tech companies are pioneering the advancement of software-defined and programmable photonic technologies. Their work includes quantum computing, chip-to-chip optical interconnects and photonic AI processors:

- IPRONICS (Spain): It develops programmable photonic processors, an integrated chip that can be altered after fabrication to execute different optical functions, similar to an FPGA in

electronics. The IPRONICS SmartLight Processor is constructed on a mesh of tunable Mach–Zehnder interferometers that can be reconfigured in real time to define the routing, filtering, or signal-processing behavior of light on the chip. This facilitates a single chip to use for multiple purposes.

- Lightmatter (USA): It develops photonics chips that use tunable interferometers and phase shifters to exhibit matrix multiplication, which is the core of AI. On March 31, 2025, it unveils "Passage™ M1000," which is a 3D active photonic interposer having the ability to deliver 114 Tbps total optical bandwidth for next-gen AI infrastructure.
- Ayar Labs (USA): Ayar Labs develops optical I/O chiplets such as "TeraPHY" to substitute electrical connections with high-speed, energy-efficient photonic connections. They are mainly working with software-defined light engine that allows for the configuration of wavelengths and channels via software, although the photonic circuit part is fixed function.
- Xanadu (Canada): It is one of the pioneering companies in the field of quantum photonic computing. Their platform "Borealis" performs quantum operations through programmable optical interferometer networks. The technology is based on continuous-variable quantum optics and programmable squeezing, displacement, and phase gates.
- IMEC (Belgium): IMEC is one of the leading companies developing waveguide mesh-based programmable photonic processors and field-programmable photonic arrays (FPPAs). They are working with a photonic compiler that can convert high-level software commands to physical configurations of photonic circuits.
- QuiX Quantum (Netherlands): Quix Quantum's Processor allows users to execute arbitrary, controlled interference between a number of optical channels, in the classical or quantum domain. Their chip features low loss, reconfigurable, temperature stable, and control software.
- LightOn (France): Optical Processing Units (OPUs) developed by LightOn for AI workloads, which is a programmable photonic chip that can perform high-dimensional computations optically, featuring faster and more energy-efficient [258].
- Ciena (Canada): Wavelogic and Reconfigurable Line System platforms by Ciena combine programmable photonic layers for optical transport networks. It allows real-time wavelength routing, signal regeneration, and reallocation of bandwidth without upgrading the hardware.
- Nexus Photonics (USA): Nexus Photonics is working with a scalable mesh architecture based on tunable phase shifters and couplers. They have expertise in designing large-scale programmable photonic integrated circuits for signal processing and AI.
- University of Twente: In collaboration with the City University of Hong Kong, the University of Twente has designed a programmable photonic chip in a thin-film lithium niobate platform. They develop a flexible chip that can process radio and light signals by integrating a TFLN modulator with a mesh of programmable components. Unlike traditional photonic circuits that have specified functionalities, this chip, like electronic chips, can be dynamically modified for various signal processing applications like electronic chips [247].

7.4 Standardization, Foundry Access, and Ecosystem Development

Scaling optical computing beyond one-off demonstrations requires three tightly coupled enablers: shared standards that make designs portable and testable, predictable access to multi-project fabrication and packaging, and an ecosystem of tools, benchmarks, and reference designs that compress iteration time. At the device and design level, interoperable process design kits (PDKs) are

the first priority. First-class support in mainstream flows—gdsfactory, IPKISS, KLayout/Cadence—should include statistical model cards, layout templates for test, and calibration utilities so that control firmware and design-for-test are developed alongside the layout, not as an afterthought.

For chiplets and co-packaged optics, harmonization with die-to-die and electrical short-reach ecosystems can reduce friction at the electronic–photonic boundary. Equally important are shared test recipes and key performance indicators that tie device behavior to application outcomes. Reliability should anchor to laser safety and photonics-specific stress tests that track insertion loss, polarization-dependent loss, resonance detuning, and RIN penalties under environmental cycling.

Packaging and I/O conventions are essential for manufacturability. Reference electrical pinouts, optical I/O maps for edge and vertical coupling, connectorization guidelines for fiber arrays and multicore fibers, and standardized alignment fiducials enable OSATs to automate assembly and screen at wafer and module level. Design-for-test and design-for-reliability layers should be present in PDKs, with keep-outs, probe access, and rework options codified.

Foundry access must broaden through MPWs across silicon, silicon nitride, indium phosphide, and heterogeneous Si/III–V bonding, supported by aggregators such as AIM Photonics, imec/ePIXfab, JePPIX, CEA-Leti, GF Fotonix, AMF, and LIGENTEC. Versioned PDKs should ship with measured variability data and example test vehicles. Qualified heterogeneous flows for wafer/die bonding, micro-transfer printing, and 2.5D/3D assemblies need standard thermal and mechanical design rules.

Finally, ecosystem development hinges on neutral, reproducible benchmarks together with open reference designs for meshes, ring banks, drivers/TIAs, and control firmware backed by golden testbenches and calibration datasets. Managed profiles for CPO and photonic chiplets should cover discovery, provisioning, calibration, health, and field updates. Investment in workforce training, open PDK access, and shared test fixtures will expand the designer base and accelerate yield learning. With coherent standards, dependable MPWs, and reusable packaging/IP, optical computing can move from bespoke prototypes to repeatable products on predictable roadmaps.

7.5 Fraunhofer Context

Fraunhofer IPMS

Fraunhofer IPMS has 2 industry standard CMOS clean rooms in Dresden, one for 200mm and one for 300mm wafer processing. The recent development of MEMS based phase shifters [259] [260] allows fully CMOS compatible phase tuning, paving an alternative approach to integrated quantum applications. Moreover, it allows more compact packaging perfectly aligning with the integrated silicon photonics scaling efforts. The 300mm clean room is currently developing a SiN platform and mitigating its challenges. As a part of the BMFTR (former BMBF) Silhouette project [261], it works on a complete value chain, paving the way to integrated silicon photonics on 300mm wafers. Its extensive knowledge about ferroelectric HfO2/ZrO2 for electronic circuits and application for neuromorphic computing shows high potential for future development and extension to PICs.

Fraunhofer HHI

Fraunhofer HHI envisions practical, manufacturable, scalable optical computing rooted in its indium phosphide (InP) foundry, which delivers multiple MPW runs and high-yield actives—SOAs, lasers, modulators, photodiodes. Complementary expertise in polymers and a low-loss silicon nitride (SiNx) process enables dense passive circuitry, delay lines, and filters. Heterogeneous InP–SiNx (with

polymers where beneficial) is central to the roadmap. A dedicated system-level program develops neuromorphic photonics, co-designing optical neural networks and nonlinear stages with electronics and control. Compact models, calibration flows, and hardware-in-the-loop training map algorithms to heterogeneous PICs and advanced packaging, including co-packaged optics. Collaborative projects—AI-NET PROTECT, 6G-RIC, SUSTAINET, GATEPOST, PHOENICS—advance 6G-ready, energy-efficient, resilient architectures and component-to-system integration from cloud to edge.

In parallel, HHI drives quantum communications across trusted-node and entanglement-based links, quantum-repeater concepts, pilot-line manufacturing, interoperability, and field trials from metro to backbone. Projects such as Q-net-Q, Quantenrepeater, SQuaD, QuNET, Qu-Pilot, QSNP, and PoLiSiQ deliver secure-network demonstrators, repeater building blocks and protocols, and integrated sources, detectors, and polarization-/phase-stable photonics. Aligning computing, networking, and quantum roadmaps—and leveraging the same heterogeneous integration—HHI targets deployable optical compute engines compatible with 6G transport, AI-native infrastructure, and European secure quantum networks.

Fraunhofer IZM

At Fraunhofer IZM, research in Optical Computing focuses on developing high-bandwidth, low-latency optical interconnects and advanced packaging solutions that enable heterogeneous integration of III-V semiconductors, silicon photonics, SiNx, glass, and control electronics on common platforms such as organics, ceramics, or PCBs. The institute also fabricates glass or silicon interposers to achieve denser I/O integration and scalable photonic integrated circuits (PICs), while leveraging SiNx and polymer technologies for ultra-low-loss passives and electro-optic functions. Their expertise extends from system-level optical computing design to advanced packaging and characterization, with flagship projects such as ALLEGRO, PROMETHEUS, FMD-QNC-Space SILC-NC, and SILHOUETTE. In Quantum Communications, IZM is advancing the miniaturization and integration of quantum photonic devices and exploring quantum sensing approaches based on NV-doped centers, SiV/Si_2V, and silicon carbide (4H-SiC) crystals. Their work also includes secure communication technologies such as quantum key distribution (QKD), post-quantum cryptography, and the use of physical unclonable functions (PUFs)—both electronic and photonic—for hardware-level security. A strong emphasis is placed on transitioning from laboratory prototypes to scalable industrial solutions, with notable contributions through projects like PROMETHEUS or ALLEGRO.

Fraunhofer XX

Chapter 8 Conclusion & Outlook

Optical computing is still at a very early stage, with numerous startups pursuing diverse approaches. Optical and quantum computing are likely to form strategies to address the rapid growth of the AI market. The shipments of the first optical processors are expected in 2027. The optical computing market is expected to grow exponentially from 2027 with a market value of $2,7B in 2034. The first shipments of photonic based quantum computers are expected not earlier than 2030, reaching a market value of $320M in 2034 [1].

Optical computing is best understood as a pragmatic partnership between light and electronics, not a wholesale replacement of digital silicon. Light excels at moving and mixing information with high bandwidth and low crosstalk. Analog photonic accelerators can target the dominant cost in AI matrix multiplications while leaving nonlinearities and state management to low-power digital blocks. Coherent meshes and wavelength-selective weight banks already demonstrate low energy consumption and low latency during inference at modest effective precision, while delay-based and integrated reservoirs deliver ultrafast equalization, control, and pattern recognition with minimal static power. Training at scale remains gated by memory bandwidth and state retention.

Scalability depends as much on manufacturing and packaging as on device physics. Silicon, silicon nitride, and III–V platforms now support repeatable multi-project wafers, while thin-film lithium niobate, phase-change materials, and 2D materials extend the design space for speed, non-volatility, and tunability. Heterogeneous bonding, micro-transfer printing, and 2.5D/3D integration tighten the electrical–optical loop and bring sources, modulators, and detectors into compact assemblies. Yet packaging and test still dominate cost and yield. Optical I/O must be standardized, thermal and mechanical stability must be engineered in from the outset, and wafer-level probe with calibrated electro-optic characterization must feed back into PDKs and compact models.

Ecosystem maturity will determine time-to-adoption. Interoperable, EDA-agnostic photonic PDKs with validated compact models, co-simulation of electro-thermal effects, and first-class hooks for control firmware are essential to increase the manufacturing capacities and speed. Manageability must converge on common discovery, telemetry, calibration, and health models so that photonic computing devices can be integrated into the existing data center infrastructure. Open benchmarks that relate energy, precision, and latency on representative workloads will let the community compare apples to apples and align research with deployable targets. Reference designs, reusable firmware, and shared calibration datasets can compress iteration cycles and broaden the designer base.

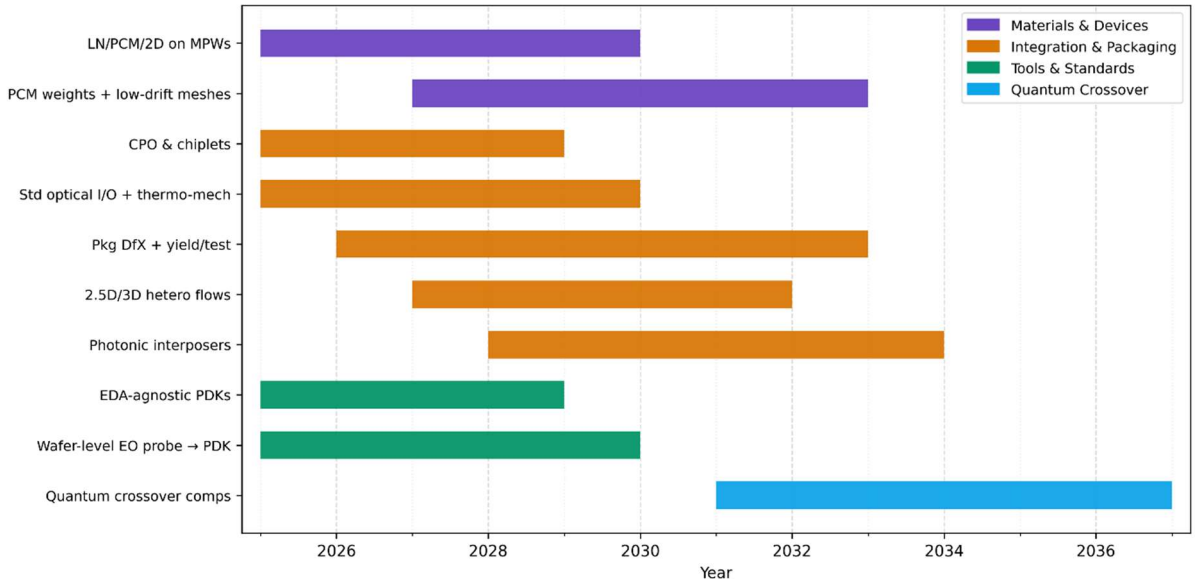

Figure 1: Technologies roadmap (2025–2036+) showing staged maturation of core enablers: Materials & Devices (LN/PCM/2D on MPWs; non-volatile analog weights), Integration & Packaging (CPO/chiplets, standardized optical I/O, qualified 2.5D/3D flows, photonic interposers, DfX/test), Tools & Standards (EDA-agnostic PDKs with wafer-level EO probe feedback), and Quantum Crossover components.

The outlook is staged. Over the next one to three years, expect CPO pilots and photonic chiplets to land in AI/HPC fabrics where power and density headroom are tight. PIC-based equalization, switching, and sensing will continue to ship in volume, and analog photonic accelerators will demonstrate application-scale inference at few-bit effective precision with credible MAC/J and latency advantages. In the three- to seven-year window, heterogeneous integration should normalize on qualified flows, phase-change weight banks and low-drift meshes will bring non-volatile analog memory closer to practice, and photonic interposers will extend optical I/O beyond chip edges. We expect MLPerf-like optical benchmarks and manageability profiles to emerge, allowing operators to plan deployments with predictable serviceability. Beyond seven years, classical and quantum photonic devices will begin to complement each other. Sources, detectors, low-loss routing, and programmable interferometers developed for quantum will benefit classical accelerators, while classical control and packaging will help scale quantum photonics. Full fault-tolerant quantum computers remain a longer-term endeavor, but quantum-inspired components like squeezed-light sources, ultra-low-noise detection, and reconfigurable meshes, will enrich classical optical computing.

Risks remain clear: memory-traffic bottlenecks and ADC/DAC overheads for mixed-signal designs, thermal drift and calibration complexity at scale, supply-chain immaturity for emerging materials, and the cost and yield burden of packaging. The remedies are equally clear: co-design algorithms to minimize data movement, elevate calibration and control to first-class design objects, drive standards and MPW access for both chips and packages, and invest in workforce training and open tooling. If the community aligns on measurable KPIs, interoperable toolchains, and manufacturable integration, optics will become a routine lever for energy, area, and latency, first in interconnect and signal processing, then in AI inference, and ultimately as a fabric where computation and communication are co-optimized by design.

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