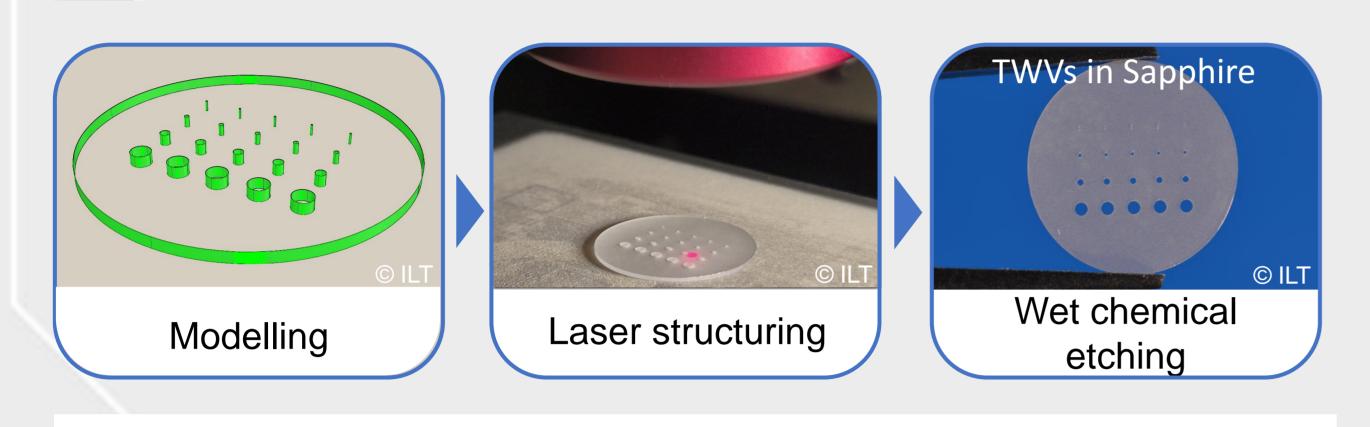


Photonics in glass

Selective laser-induced etching (SLE) and packaging

1 Selective Laser-Induced Etching (SLE)



SLE-Process for creating 3D structures from transparent dielectrics (for example: fused silica, BOROFLOAT, sapphire)

1. Modeling

 Slicing of the CAD model and calculation of laser vectors along the component surface

2. Laser structuring

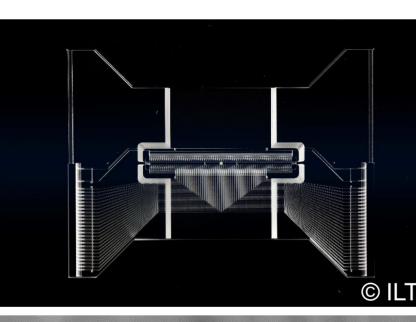
Structuring of modification lines within the transparent material using tightly focused USP laser radiation

3. Wet chemical etching

• Etching of the modified areas using KOH or HF

Special features & application examples

- Almost unlimited freedom of geometry
- High precision (<1 μm)
- Surface roughness:
- After SLE: Sa < 1 µm
- After laser polishing: Sa < 10 nm
- High degree of flexibility (digital process)



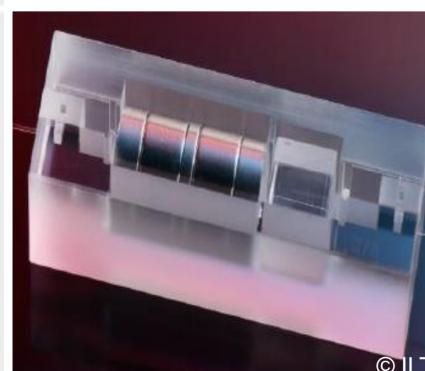
Ion traps (ATIQ)

Glass-based ion traps with **in-volume structuring** (undercuts) and three-dimensional electrode design.



Microresonators (LAR3S)

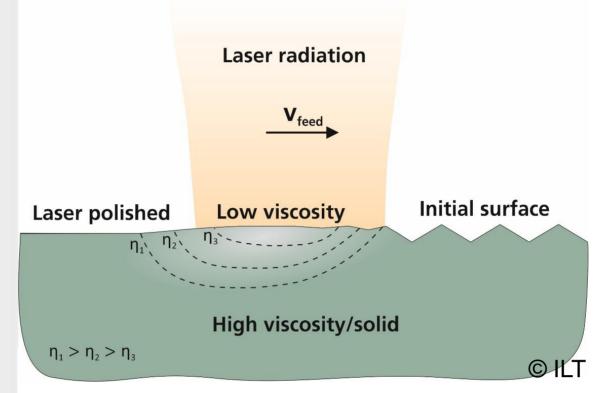
Glass structures with **low surface** roughness for storing light of specific wavelengths. The dimension of the structure is $\sim 100 \ \mu m$ (disc) to $\sim 50 \ \mu m$ (base).



Fiber chip coupler (HIPEQ)

Optical connection element with fiber clamp and holder for the installation of microoptics. The dimensions of the component are $2.85 \times 1 \times 1 \text{ cm}^3$ with a **fabrication tolerance** of **<200 nm (optics mounts)**.

Combined process SLE + glass polishing



- Absorption of laser radiation close to the surface (< 30 μm)
- Local reduction in viscosity leads to redistribution of material due to its surface tension
- > Ablation-free polishing process

Areas of application:

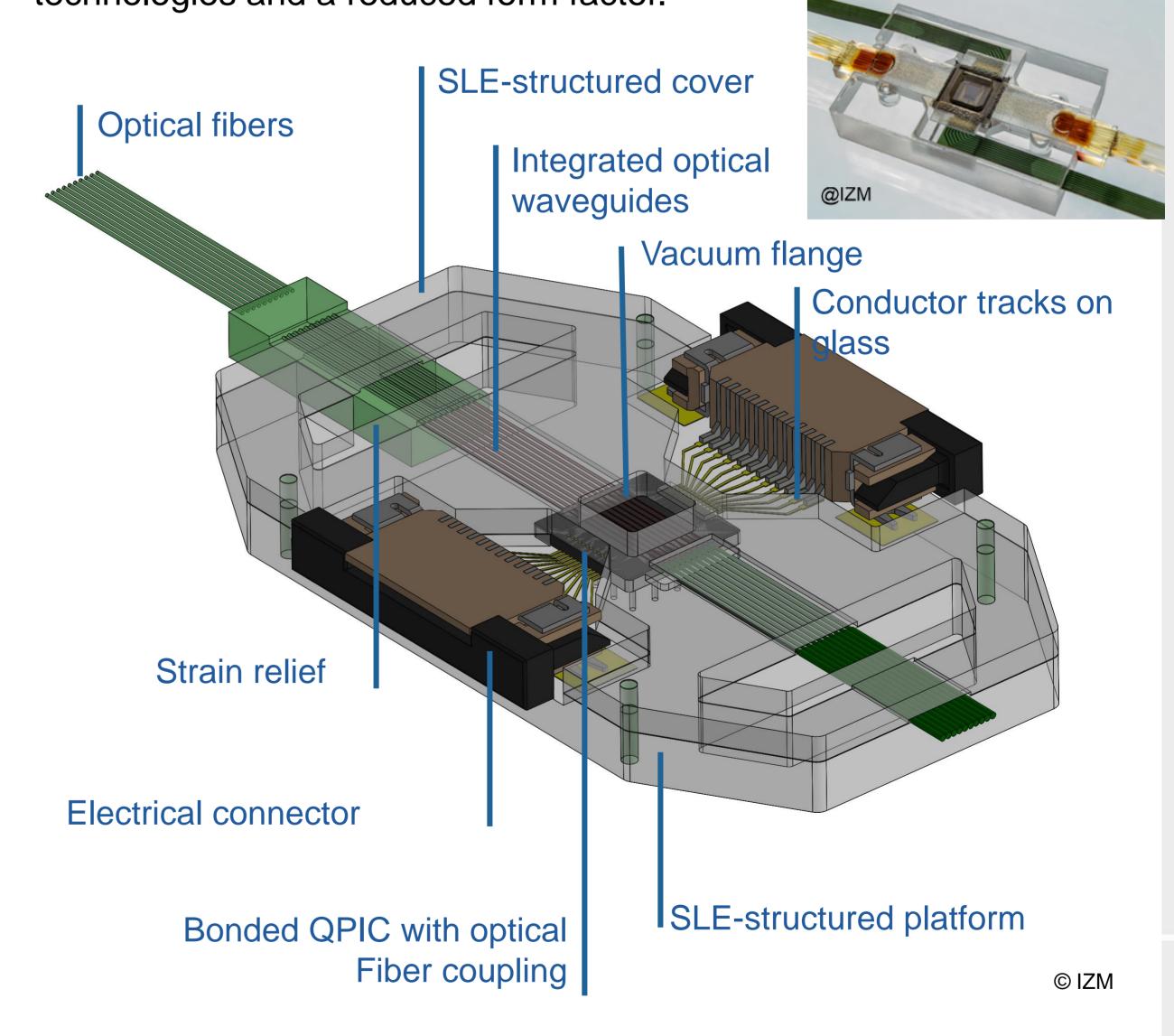
- Polishing of ion trap electrodes to reduce background noise
- Production of optical components (e.g. special/micro-optics, integrated optics)



After CO₂ polishing:

4 Generic test packaging platform

Quantum photonic PIC (QPIC) must be optically and electrically contacted and often connected to vacuum recipients. A glass-based **test platform** is offered for the development stage. The final product package can later be manufactured in quantities using the same technologies and a reduced form factor.







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