

Biologically inspired systems in silicon

Neuromorphic hardware architectures and their design



Building blocks, architectures and processors

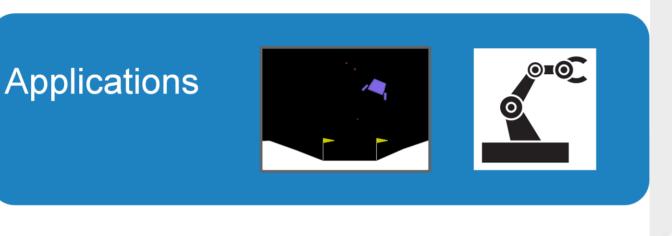
Novel neuromorphic devices and hardware architectures inspire the design of processors with previously unreached energy efficiency or latency characteristics.

Within the **FMD** we combine know-how on all abstraction levels of neuromorphic computing to enable the design of **neuromorphic processors.**

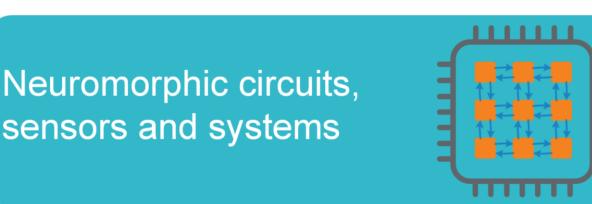
Solving consumer and industrial problems

> Enabling applications

Integration and scaling



Neuromorphic algorithms



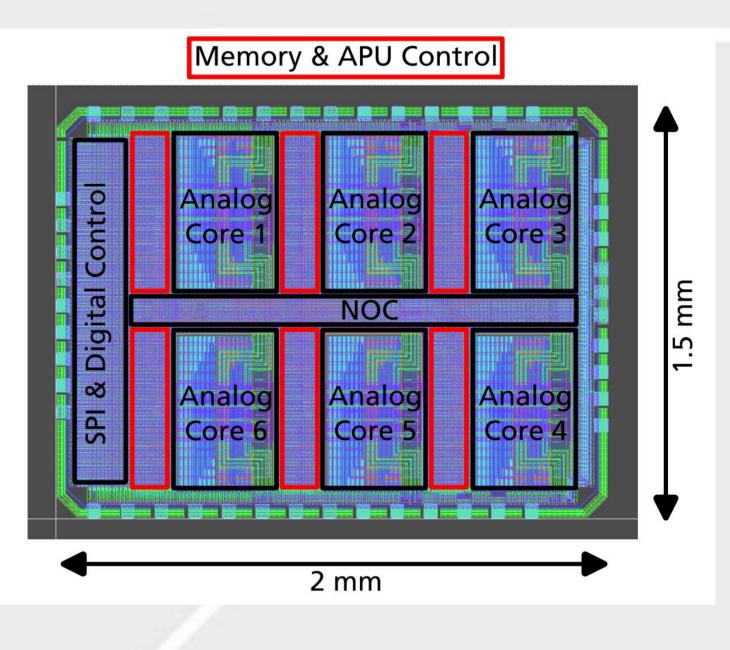
We combine enabling building blocks and neuromorphic devices into architectures to design processors for different algorithms and applications.

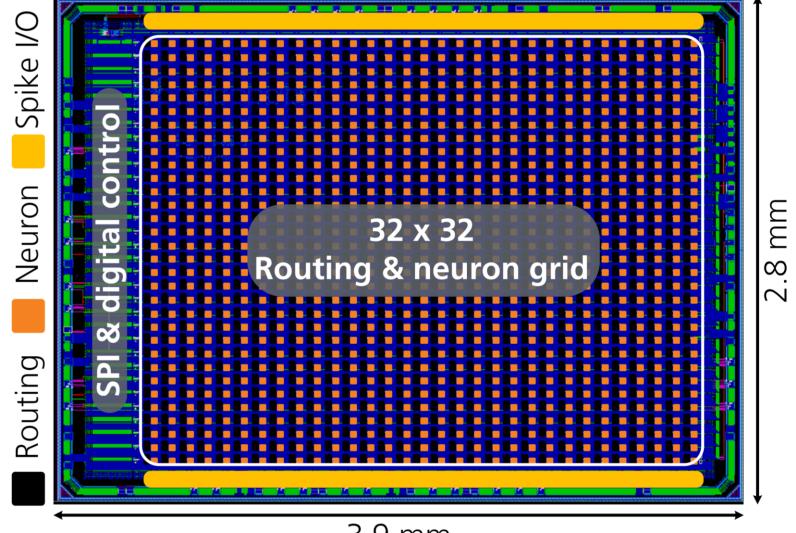
ADELIA

- Packet-switched Network-on-Chip for high flexibility and multi-byte communication
- Analog in-memory computing processing cores for multiply-accumulate (MAC) operations
- Few but complex analog processing unit (APU) cores
- For Artificial Neural Networks (ANNs)
- USP: Ultra-low power

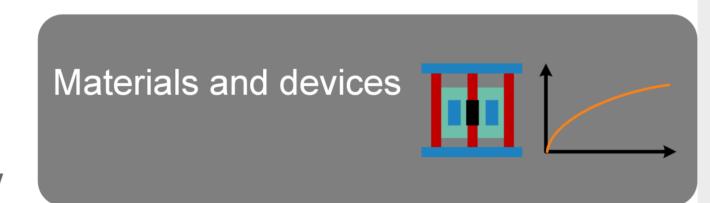
SENNA

- Circuit-switched Network-on-Chip for ultra-fast single-spike routing
- Leaky-integrate-and-fire (LIF) neuron processing cores
- Many but simple spike processing node (SPN) cores





Exploring the future beyond CMOS



- For Spiking Neural Networks (SNNs)
- USP: Ultra-low latency

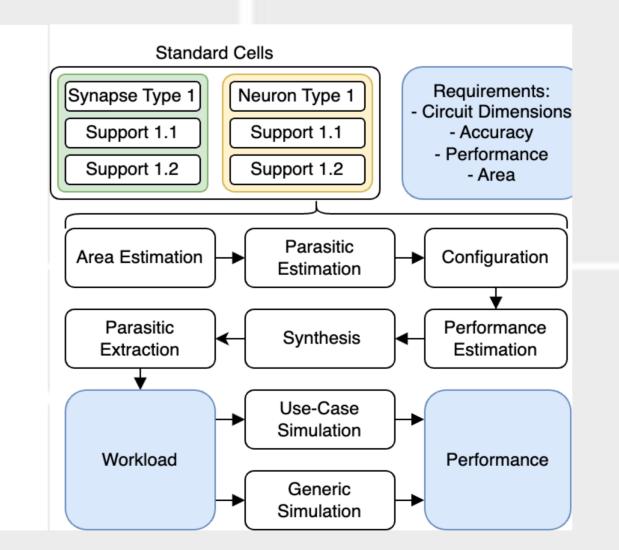
3.9 mm

Efficient design flows 3

Design automation for large-scale analog design

- Integrates into industry standard design flow and tools for analog/mixed-signal circuits
- Leverages custom analog standard-cells for best performance and flexibility
- Fully automated assembly of module level circuits
- Fully automated simulation and verification
- Enables design automation of **analog computing**





analog

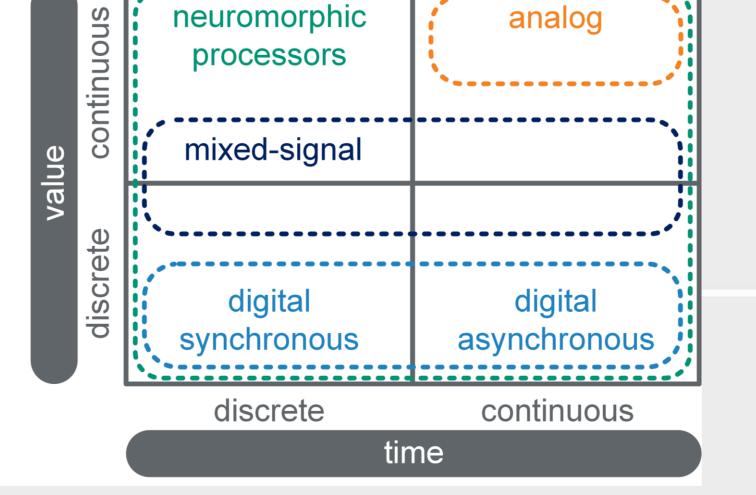
Enabling design 4

We enable the design of neuromorphic hardware with

- IP and custom designs of enabling building blocks like ADCs,
- our experience in HW/SW co-design and architecture exploration.
- our efficient design flows for analog, mixed-signal and mixed-timing hardware.

Enabling applications 5

- Exploit commercial design tools for synchronous digital circuits for place and route and Static Timing Analysis (STA)
- Hide asynchronous timing in custom digital cells
- Hide mixed-signal circuits under digital interfaces
- Enables design automation of **spiking processors**



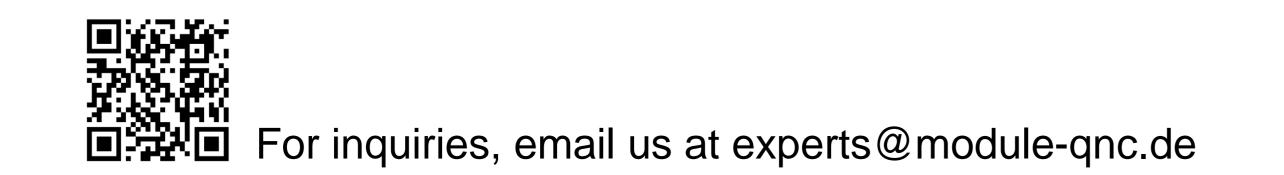
neuromorphic

processors

Do conventional processors limit your applications?

Get in touch to explore our neuromorphic processors as alternatives.





Federal Ministry of Education and Research