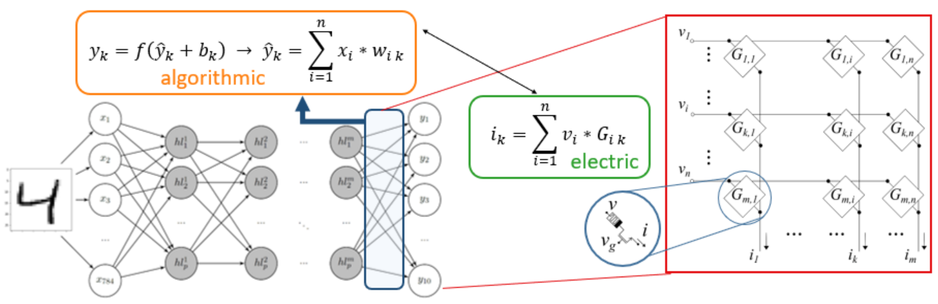
New technology approaches for neuromorphic computing

Memristor applications: In-memory computing in crossbar architecture

1 In-Memory Computing

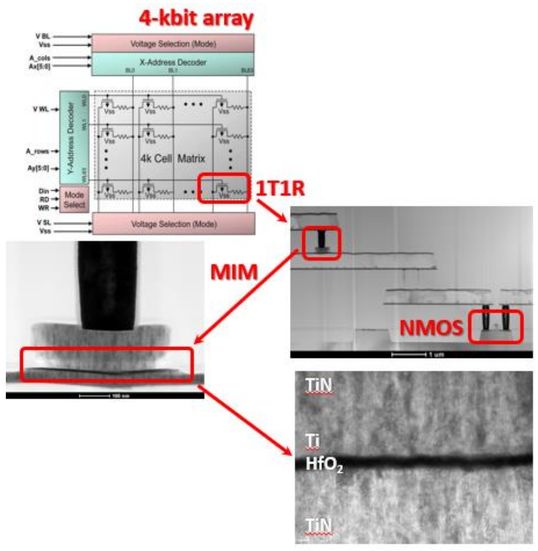
Most of the power consumption in AI accelerators is due to the well-known memory wall problem.

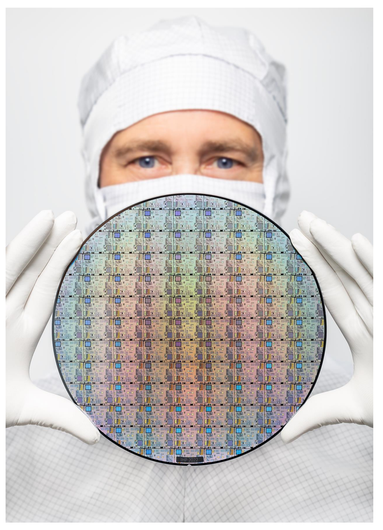
Solution: In-memory computing; the data is computed where it is stored.



2 200 mm CMOS RRAM Technology

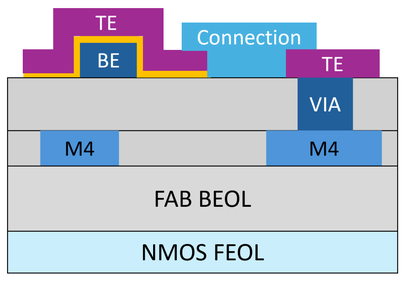
CMOS integrated 4 Kbit test array with peripheral drive electronics, developed in the 130 nm technology node of the IHP.

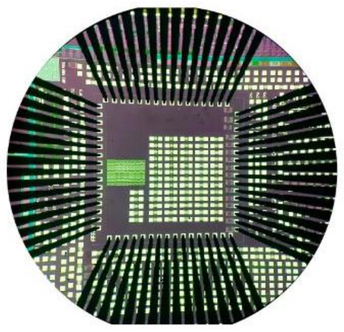




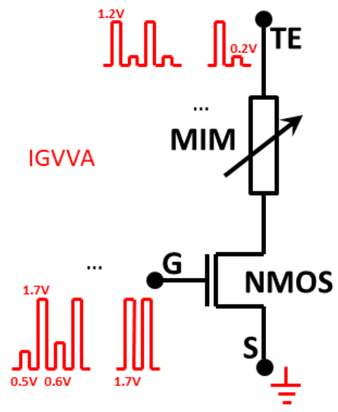
3 Half-adder Implementation with RRAMs

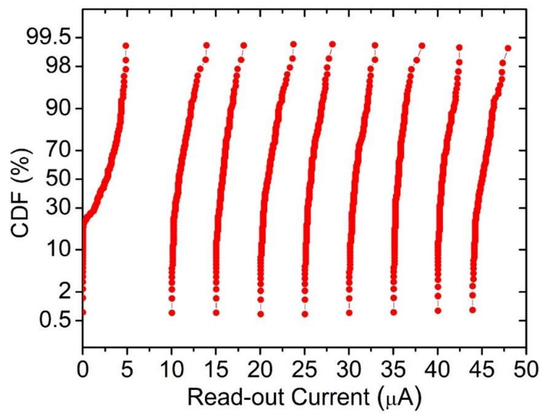
Integration of TaOx/Ta-RRAM on a CMOS substrate and realization of a half adder in 31x16 crossbar array using in-memory computing.



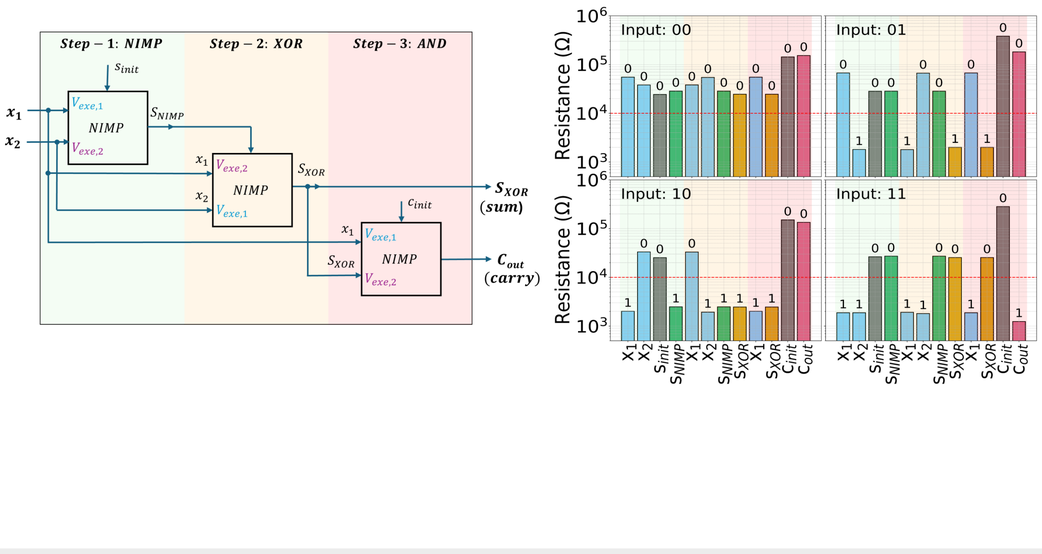


Verified algorithms for programming multiple conductive states in the individual memristive devices.





4 Outlook



Making a process line for next-generation neuromorphic systems co-integrated with CMOS platform available:

- Extension of the existing IHP process environment for the targeted expansion of the structuring capabilities of the integrated RRAM devices.
- Extension of the existing 200 mm silicon cluster by the components metal PVD, metal oxide PVD and handler, for the deposition of analog switchable RRAM devices.

For inquiries, email us at experts@module-qnc.de

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